Fig. 1

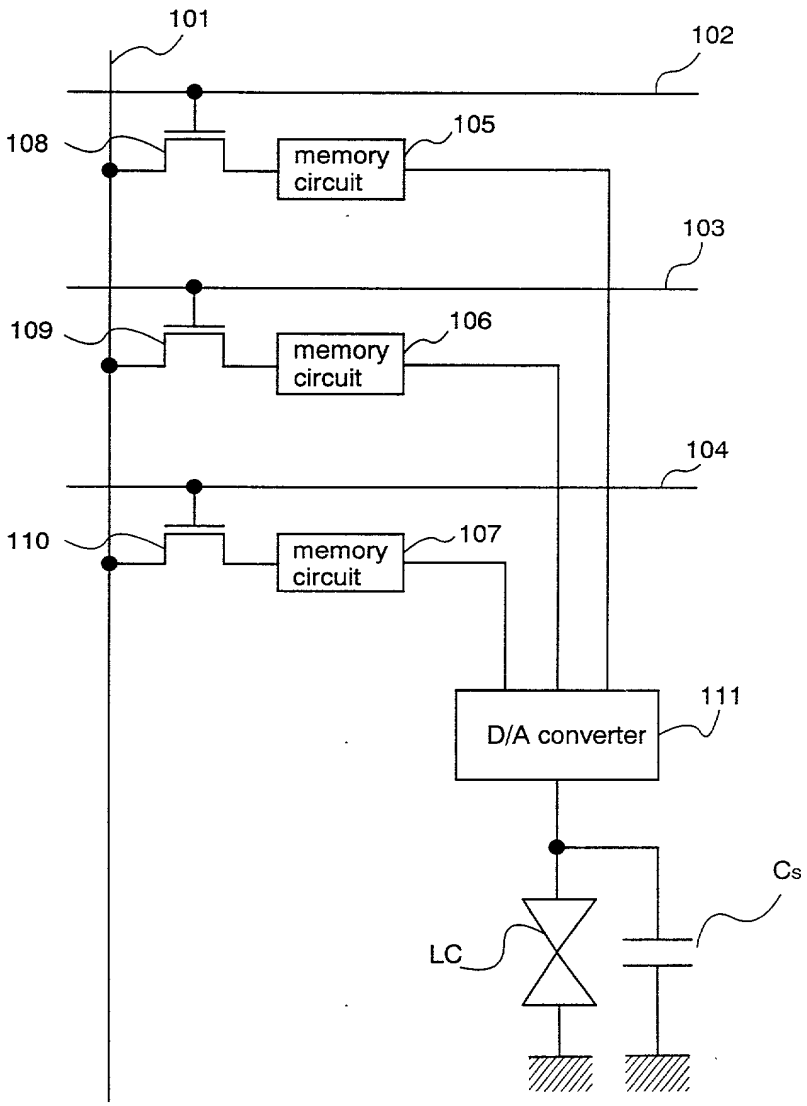

101
102
108
105
memory circuit
103
109
106
memory circuit
104
110
107
memory circuit
111
D/A converter
Cs
LC

Fig. 2

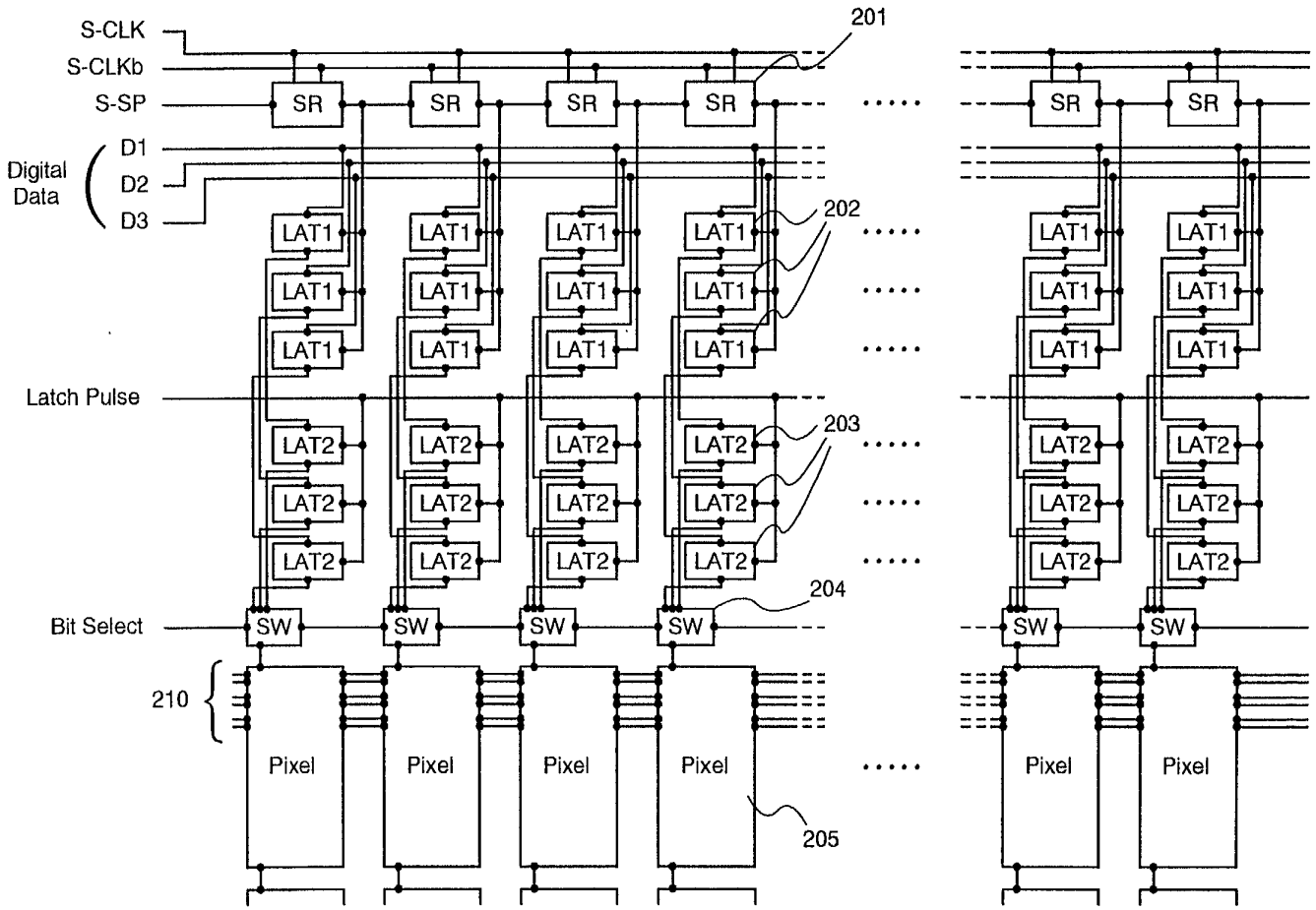

S-CLK
S-CLKb
S-SP
Digital Data
D1
D2
D3
Latch Pulse
Bit Select
210
SR
LAT1
LAT2
SW
Pixel
201
202
203
204
205

Fig. 3A

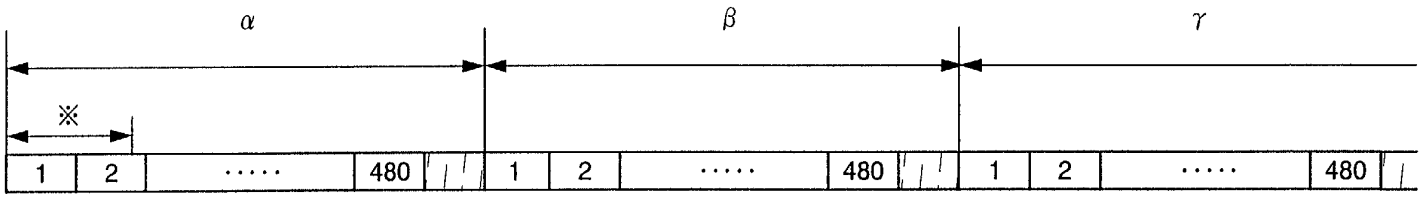

α
β
γ
※
1
2
·····
480
1
2
·····
480
1
2
·····
480

Fig. 3B

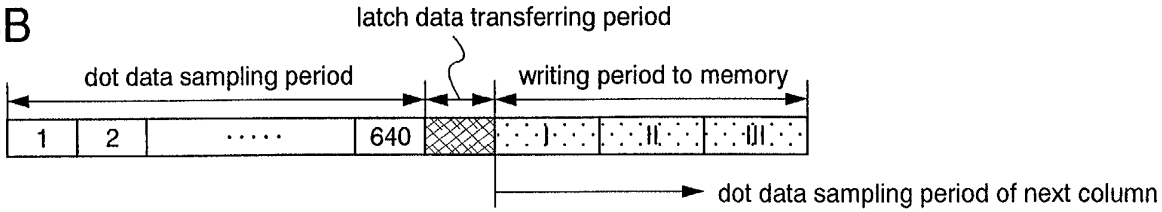

latch data transferring period
dot data sampling period
writing period to memory
1
2
·····
640
dot data sampling period of next column

Fig. 4

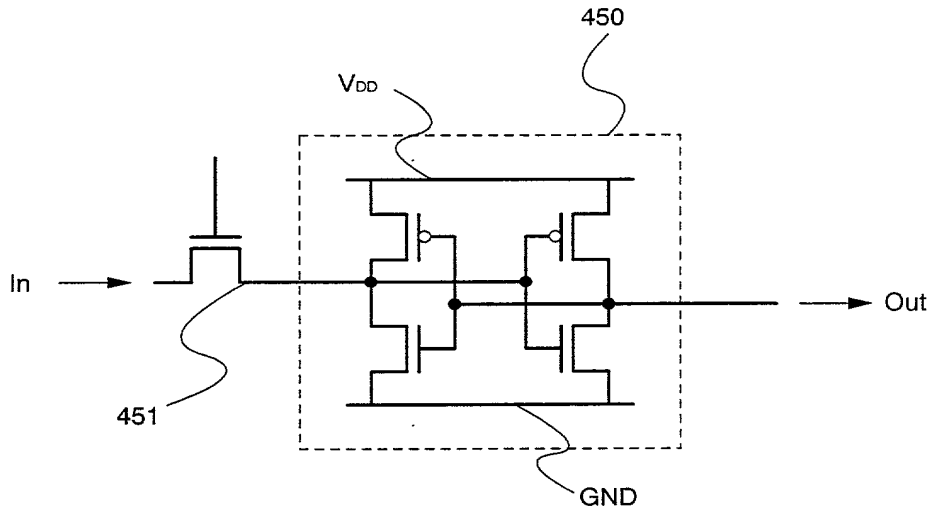


Fig. 5

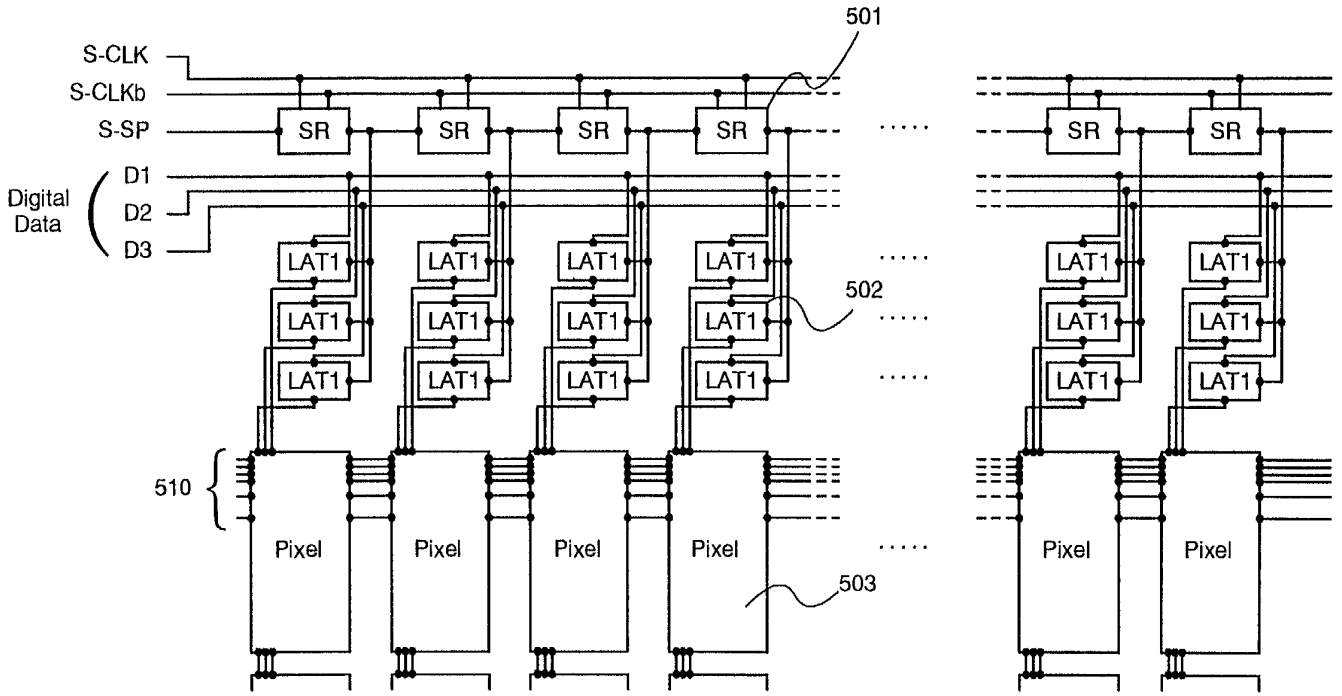

501
S-CLK
S-CLKb
S-SP
Digital Data
D1
D2
D3
SR
LAT1
502
510
Pixel
503

Fig. 6

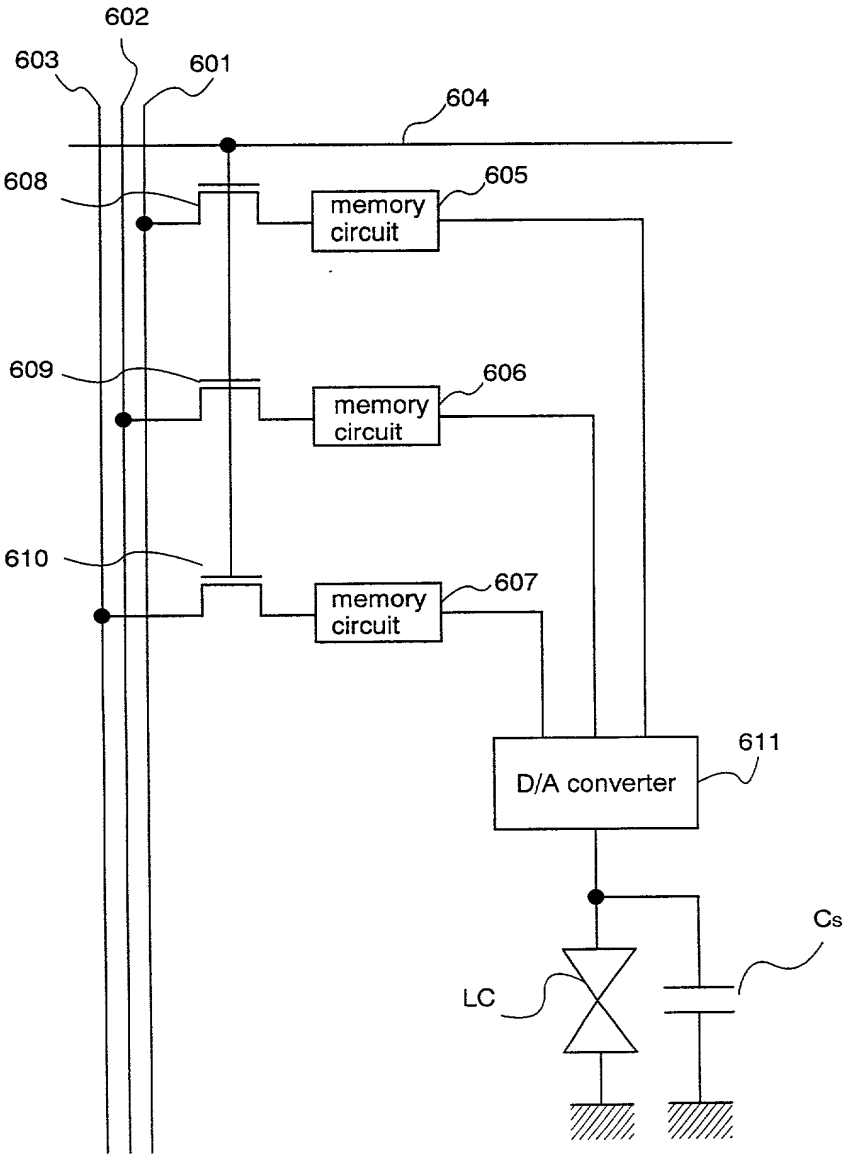

602
603
601
604
608
605
memory circuit
609
606
memory circuit
610
607
memory circuit
611
D/A converter
Cs
LC

Fig. 7A

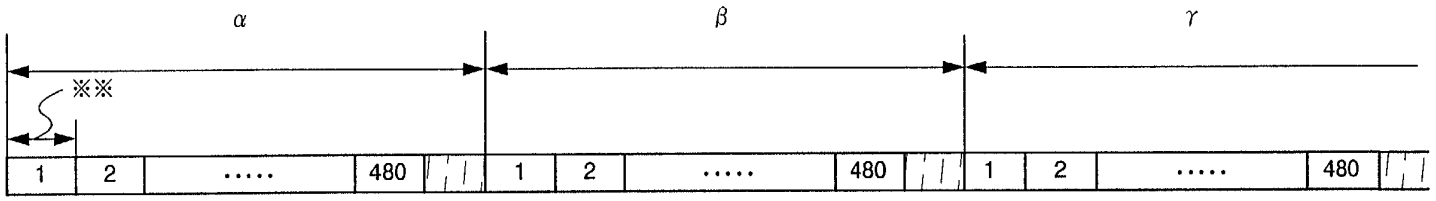

α
β
γ
※※
1
2
.....
480
1
2
.....
480
1
2
.....
480

Fig. 7B

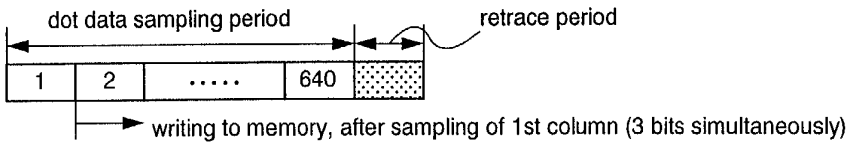

dot data sampling period
retrace period
1
2
.....
640
writing to memory, after sampling of 1st column (3 bits simultaneously)

Fig. 8

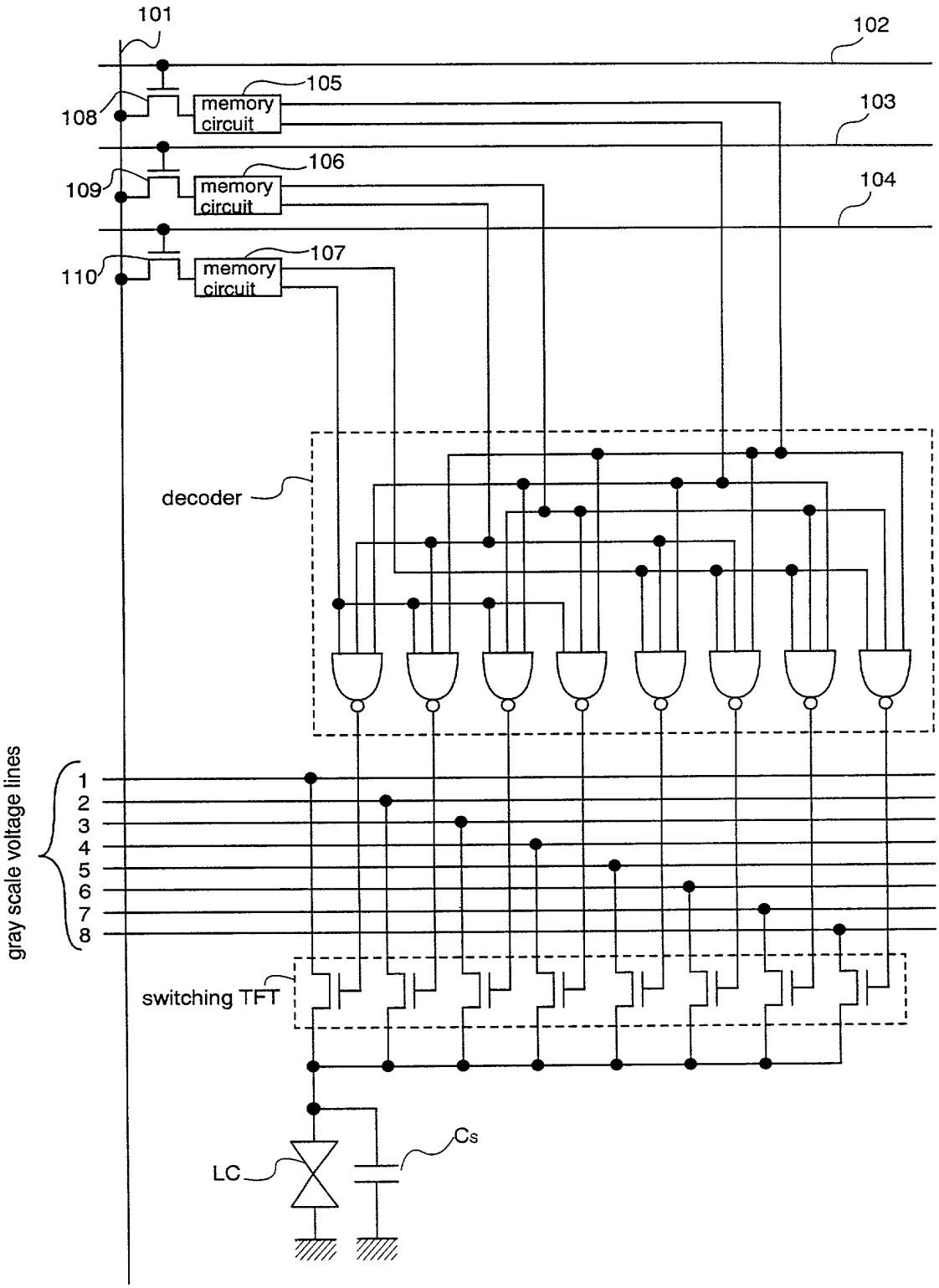

101
102
105
memory circuit
108
103
106
memory circuit
109
104
107
memory circuit
110
decoder
gray scale voltage lines
1
2
3
4
5
6
7
8
switching TFT
Cs
LC

Fig. 9

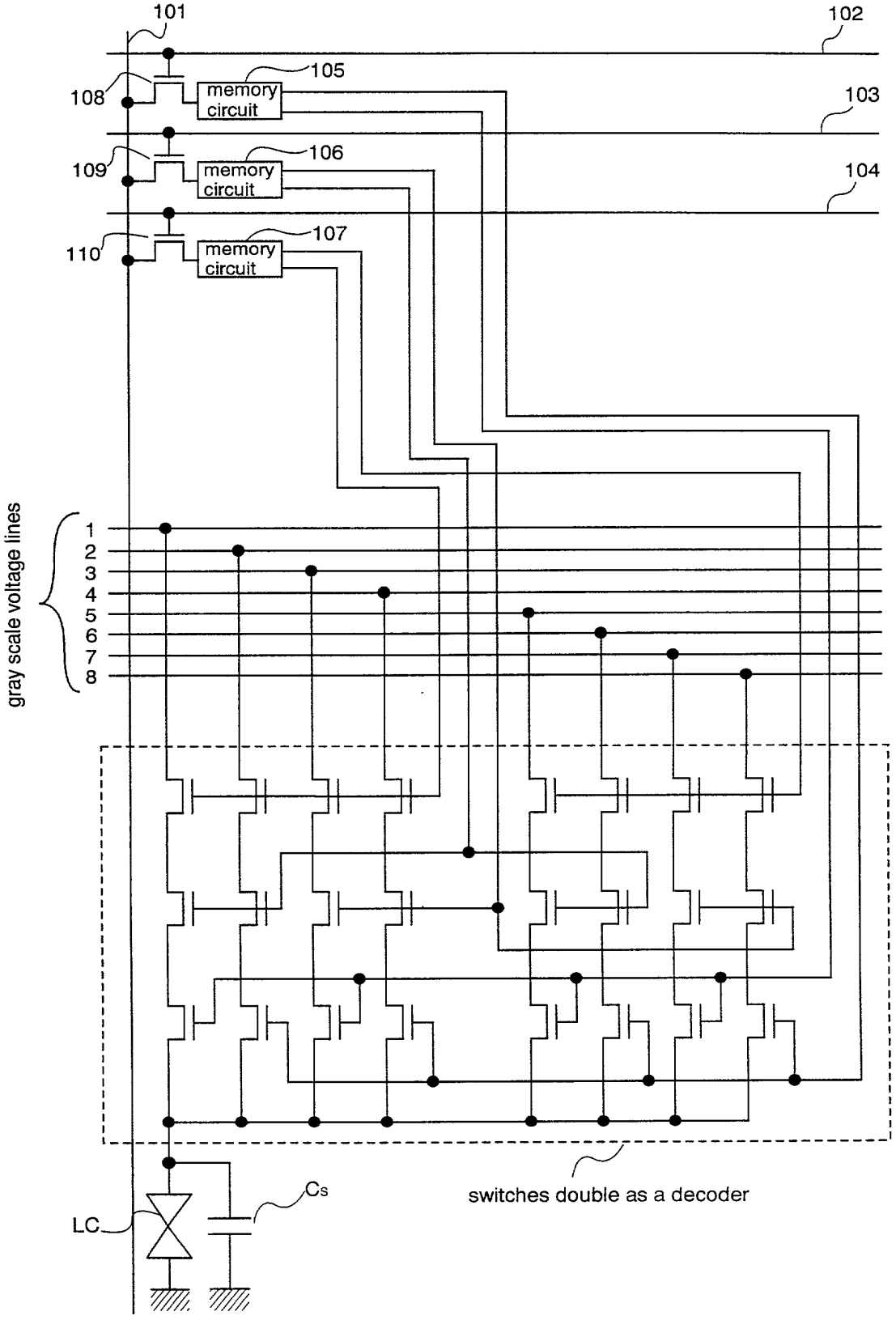

101
102
105
memory circuit
108
103
106
memory circuit
109
104
107
memory circuit
110
gray scale voltage lines
1
2
3
4
5
6
7
8
switches double as a decoder
Cs
LC

Fig. 10A

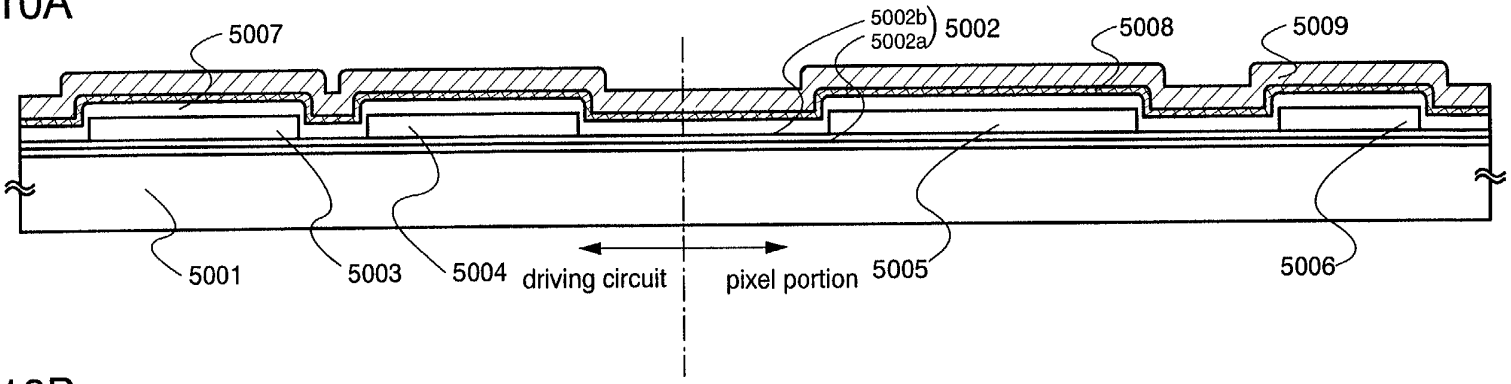


Fig. 10B

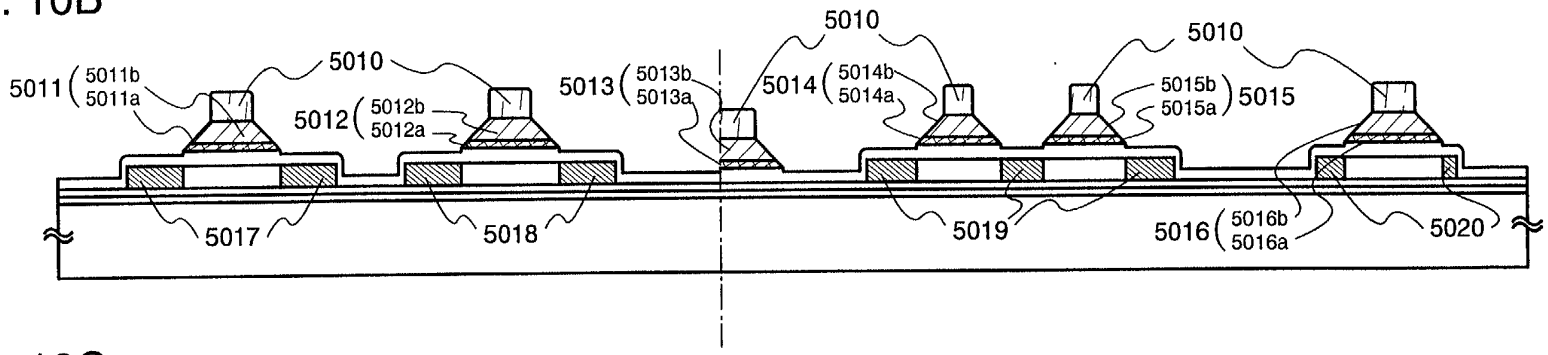


Fig. 10C

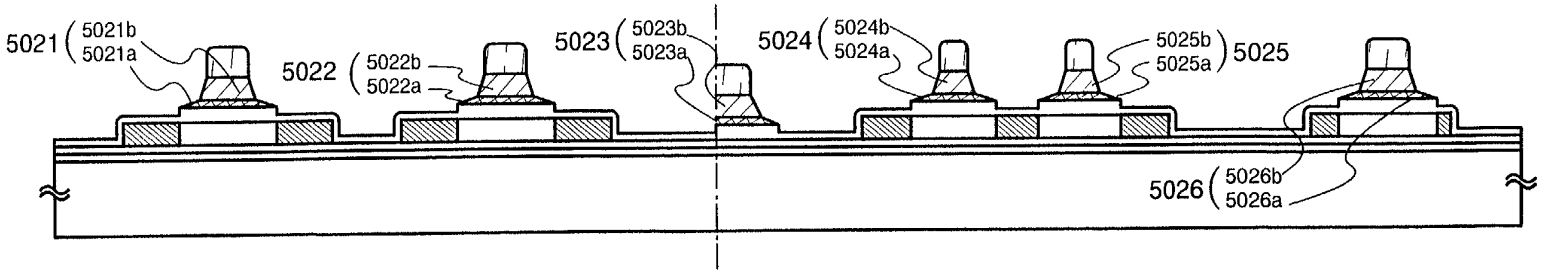


Fig. 11A

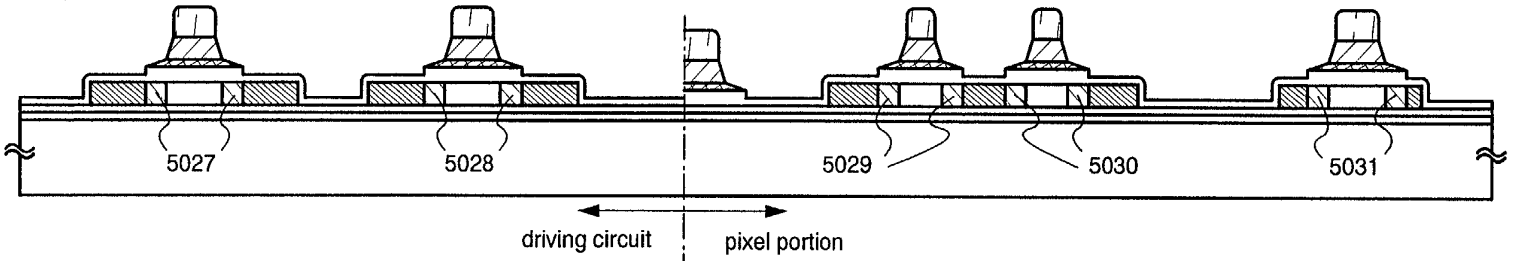


Fig. 11B

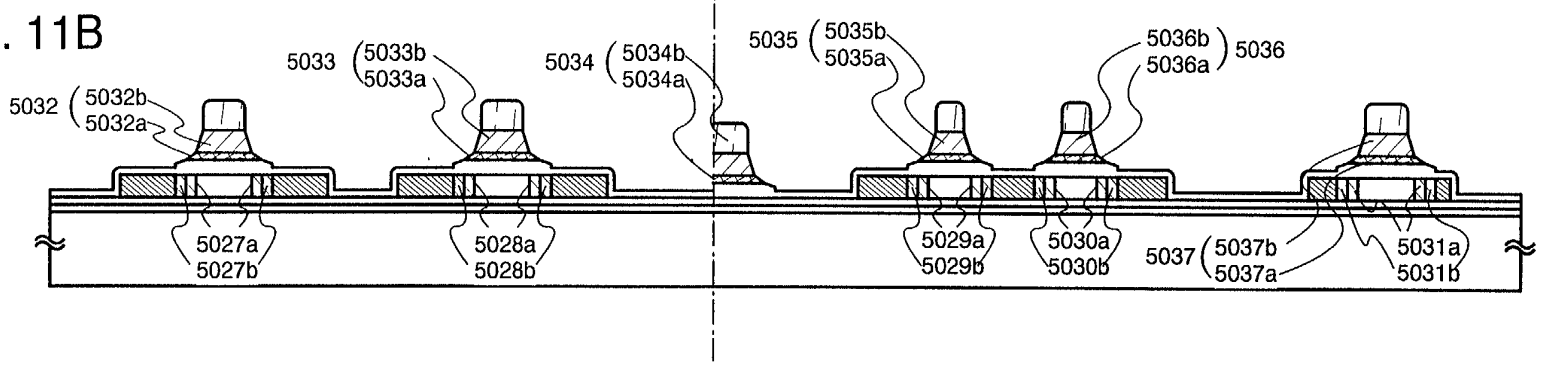


Fig. 11C

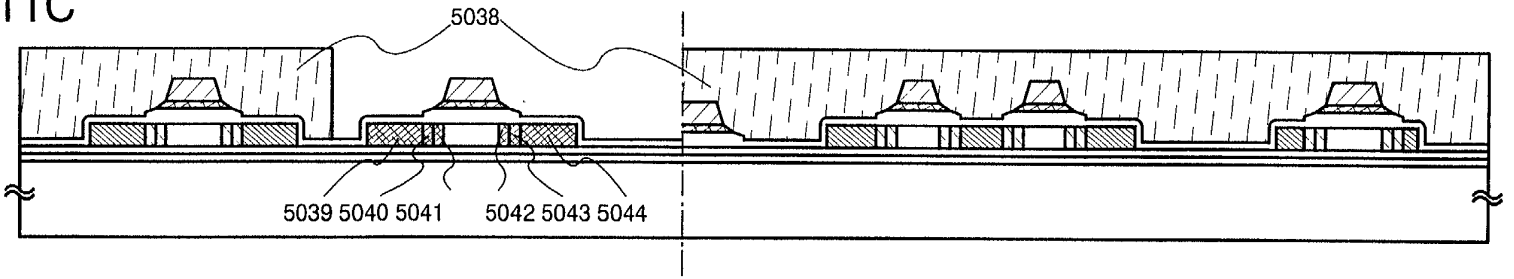


Fig. 12A

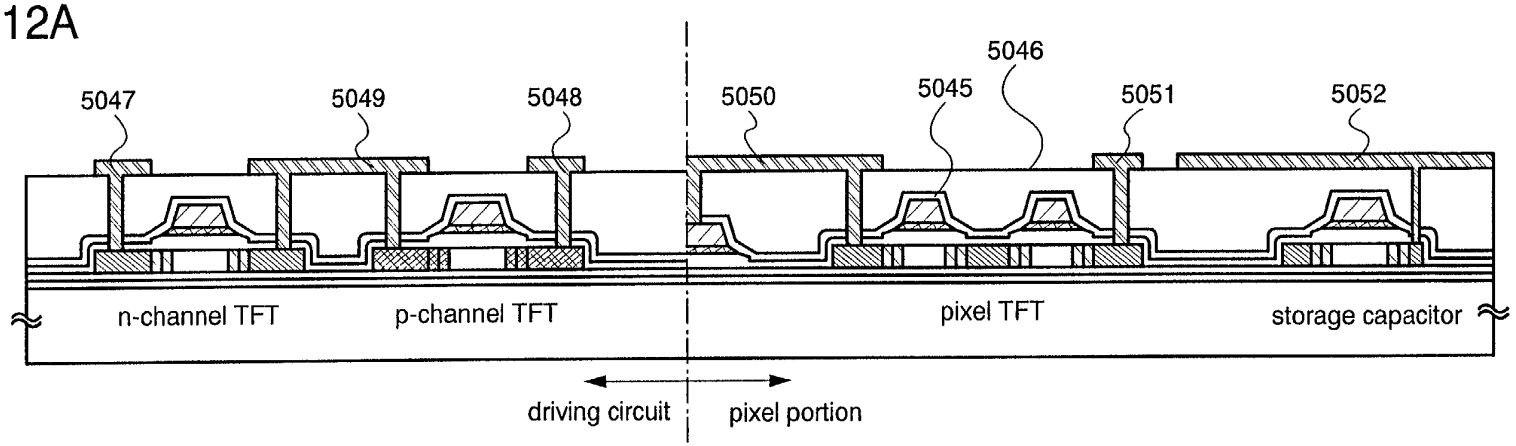


Fig. 12B

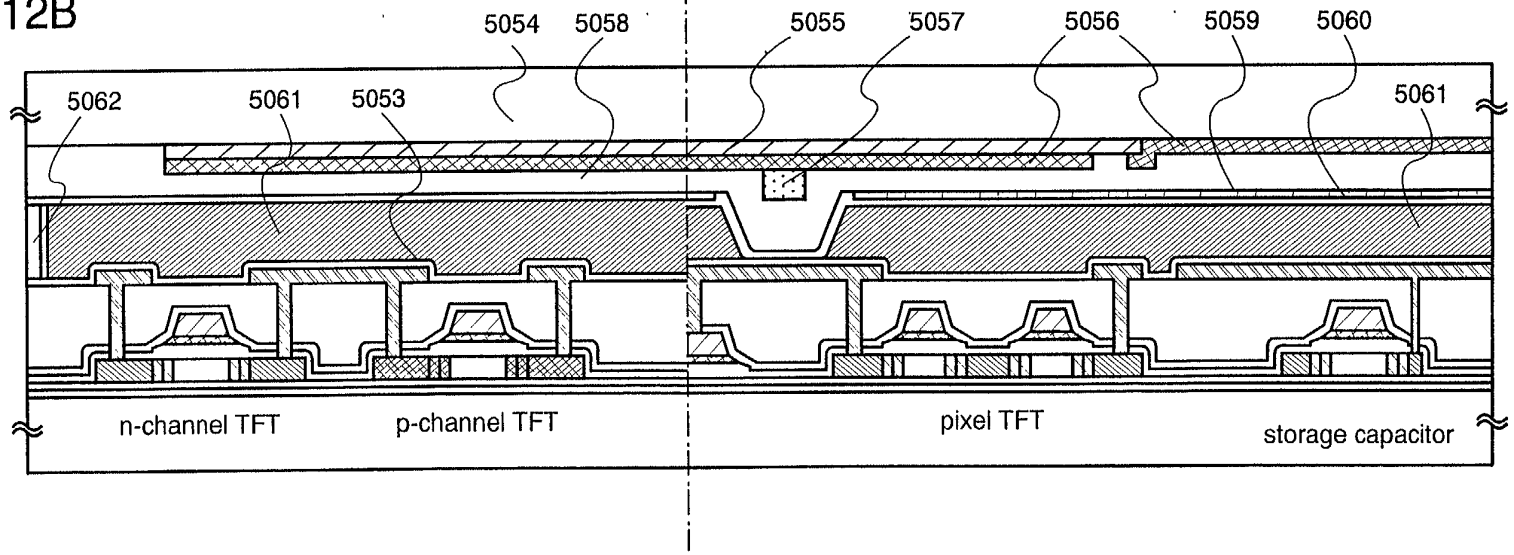


Fig. 13

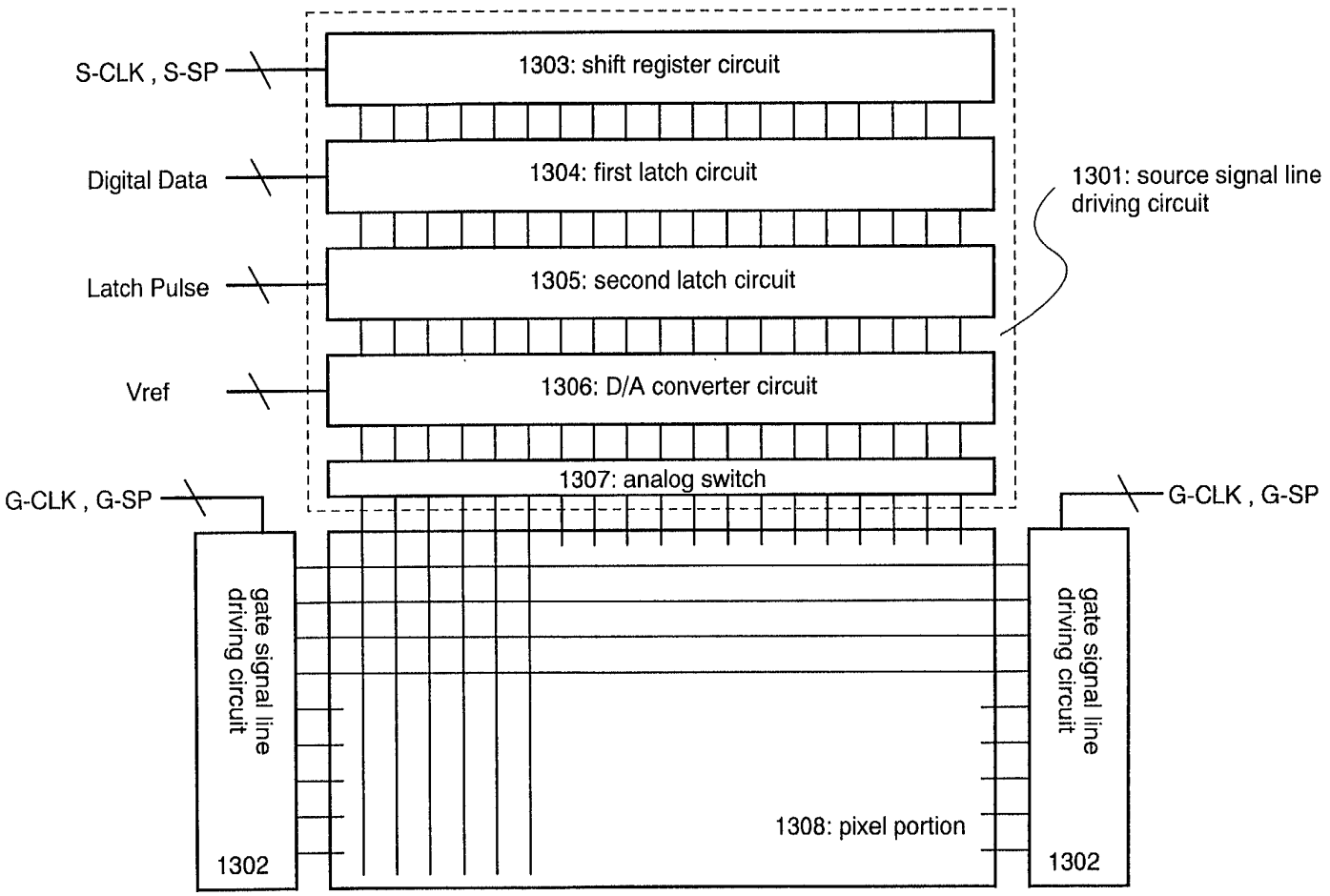
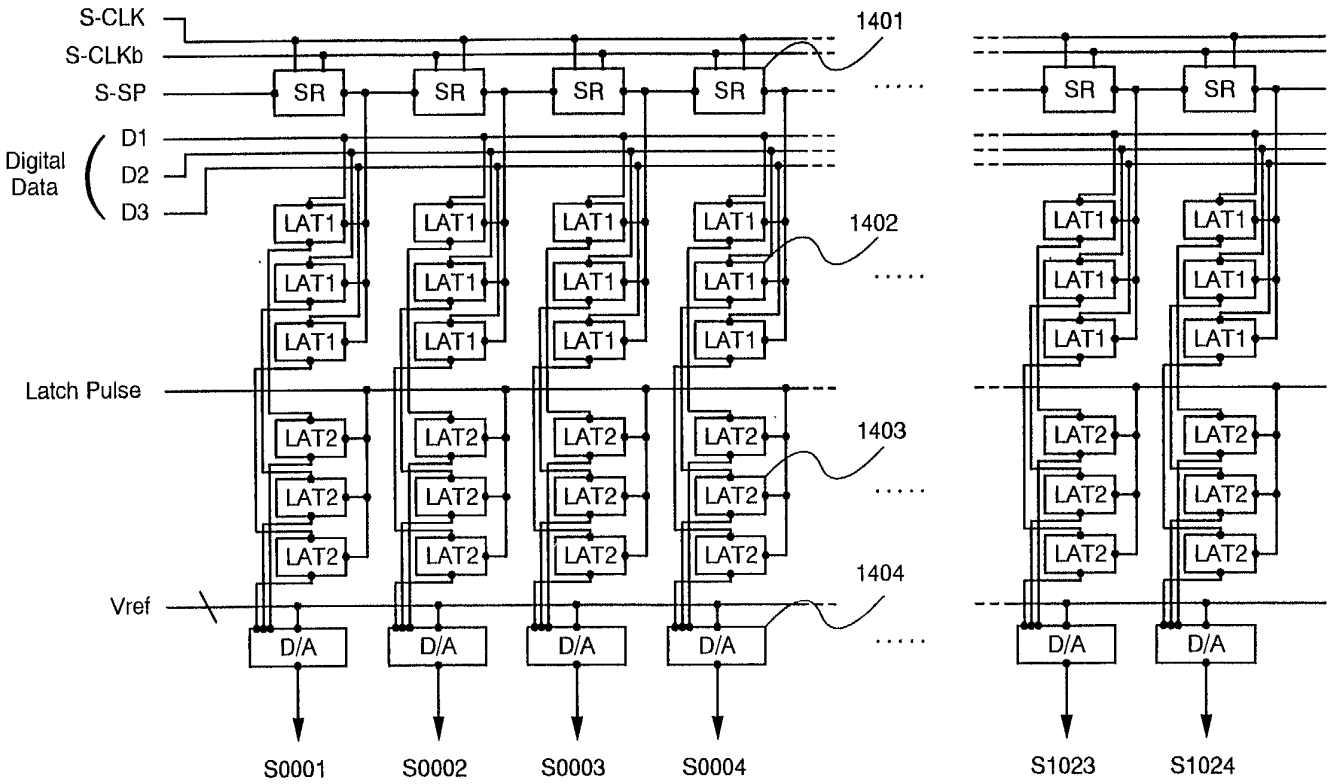

S-CLK , S-SP
1303: shift register circuit
Digital Data
1304: first latch circuit
1301: source signal line driving circuit
Latch Pulse
1305: second latch circuit
Vref
1306: D/A converter circuit
1307: analog switch
G-CLK , G-SP
G-CLK , G-SP
gate signal line driving circuit
gate signal line driving circuit
1308: pixel portion
1302
1302

Fig. 14



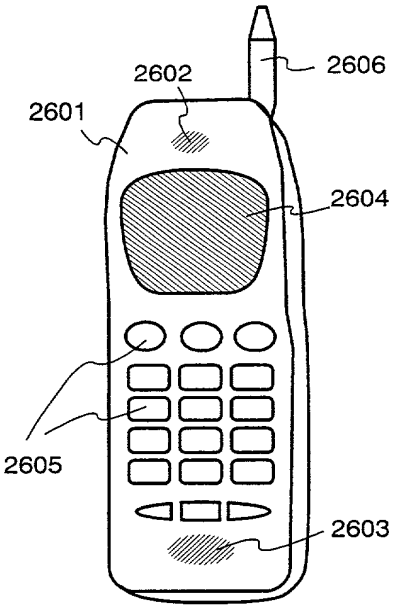


Fig. 15A

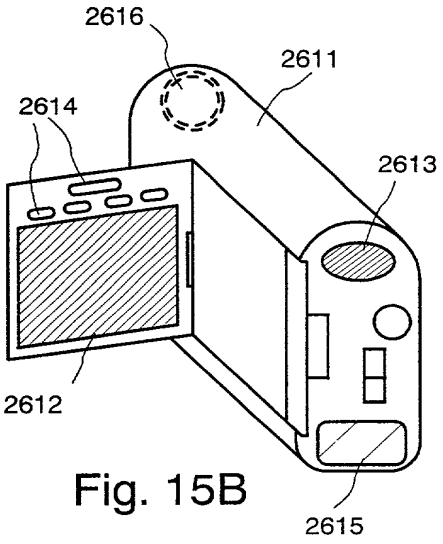


Fig. 15B

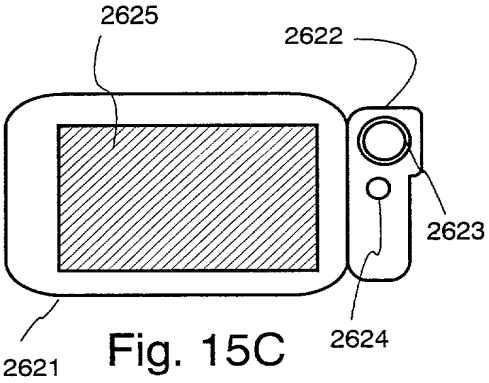


Fig. 15C

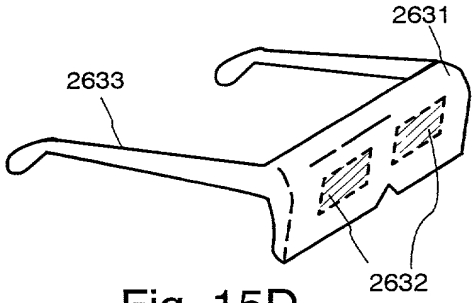


Fig. 15D

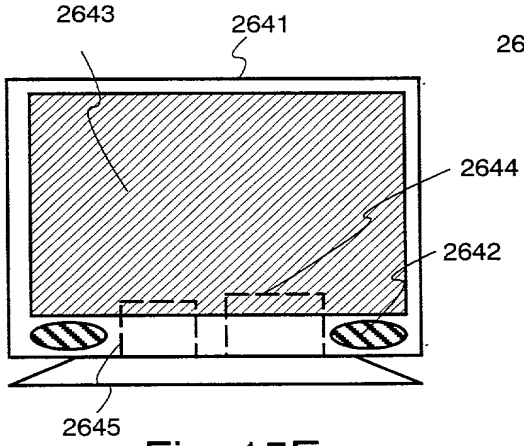


Fig. 15E

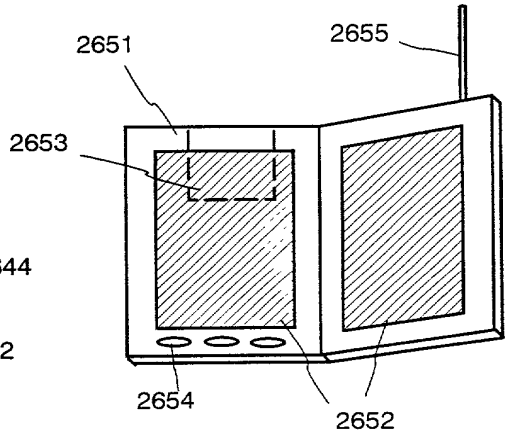


Fig. 15F

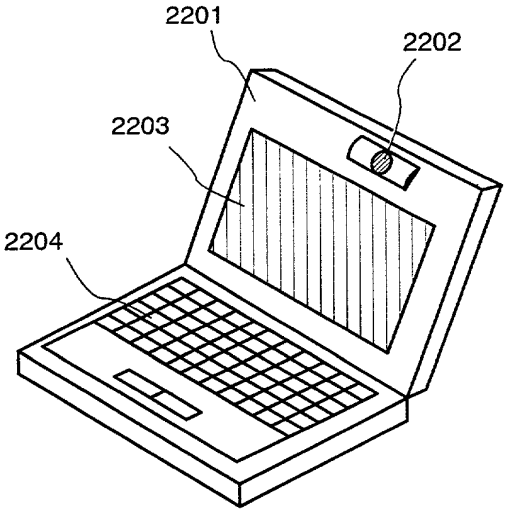


Fig. 16A

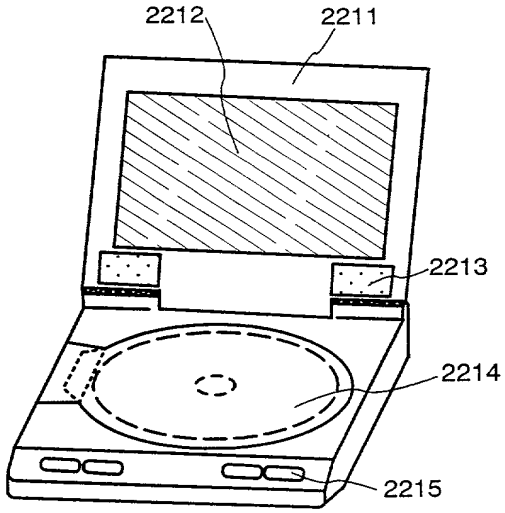


Fig. 16B

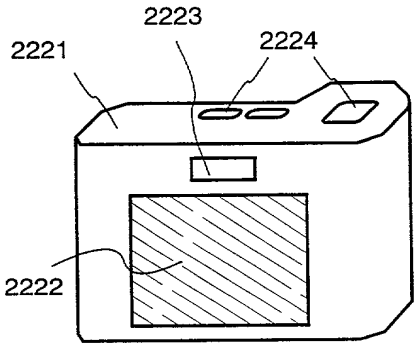


Fig. 16C

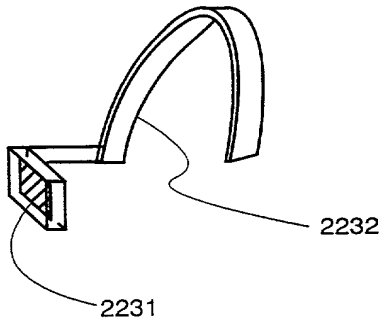


Fig. 16D

Fig. 17

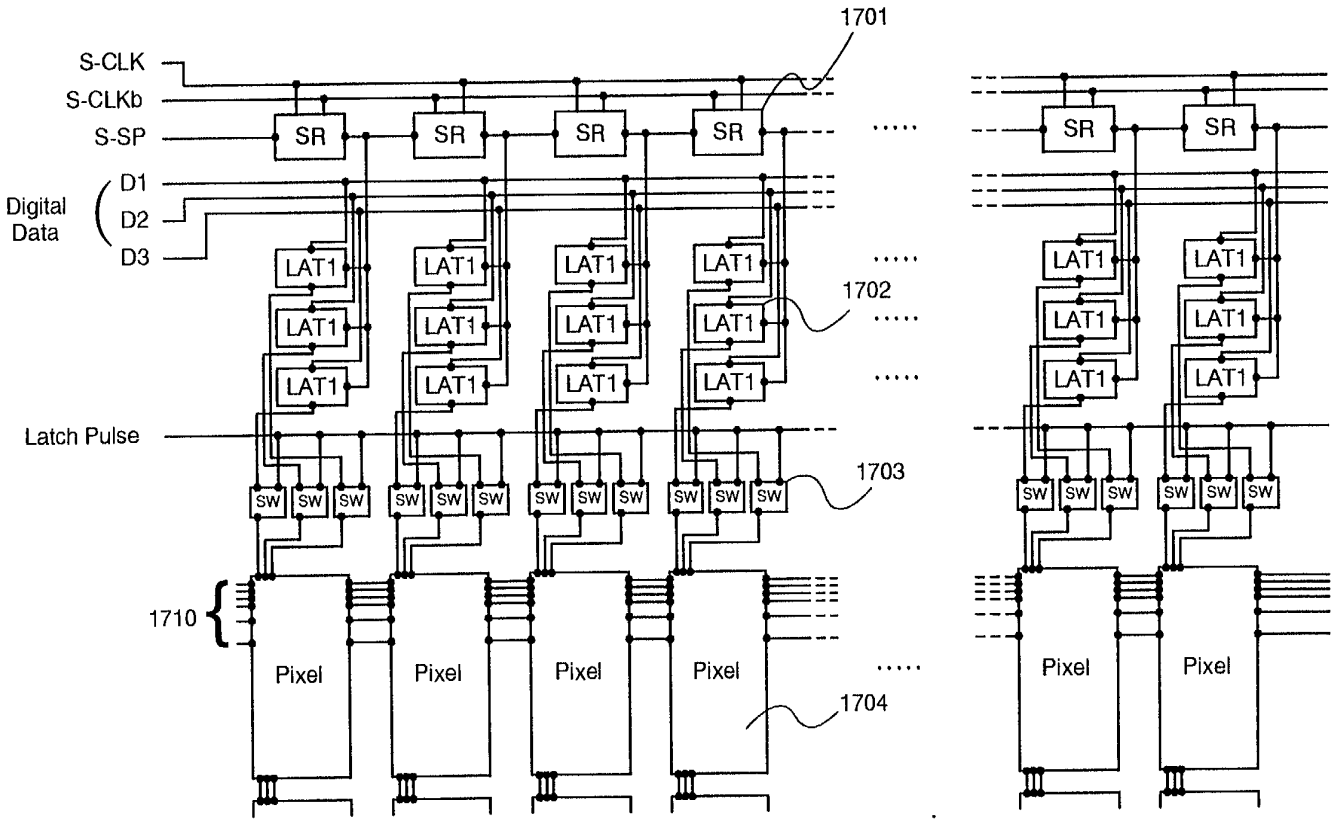

1701
S-CLK
S-CLKb
S-SP
Digital Data
D1
D2
D3
SR
LAT1
1702
Latch Pulse
SW
1703
1710
Pixel
1704

Fig. 18A

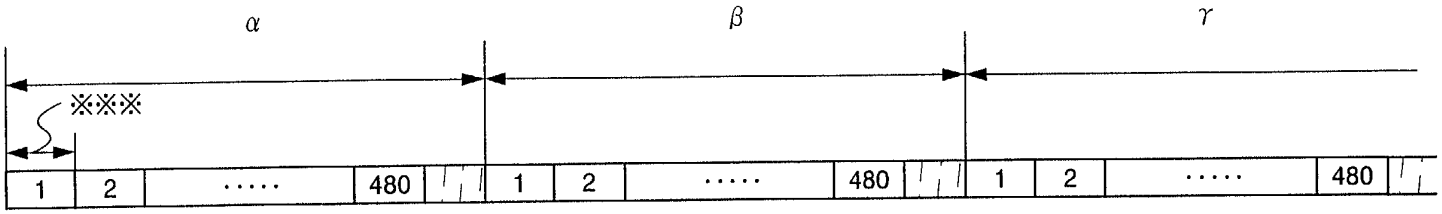


Fig. 18B

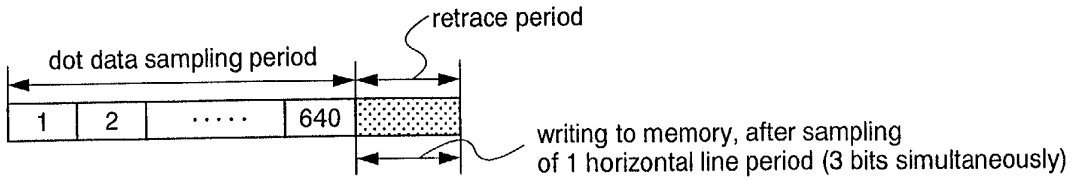


Fig. 19A

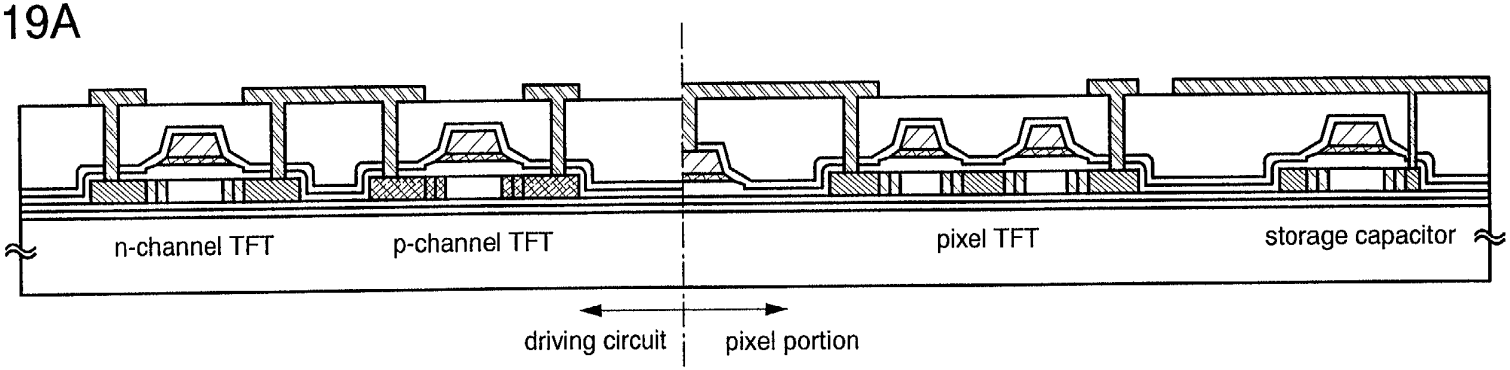


Fig. 19B

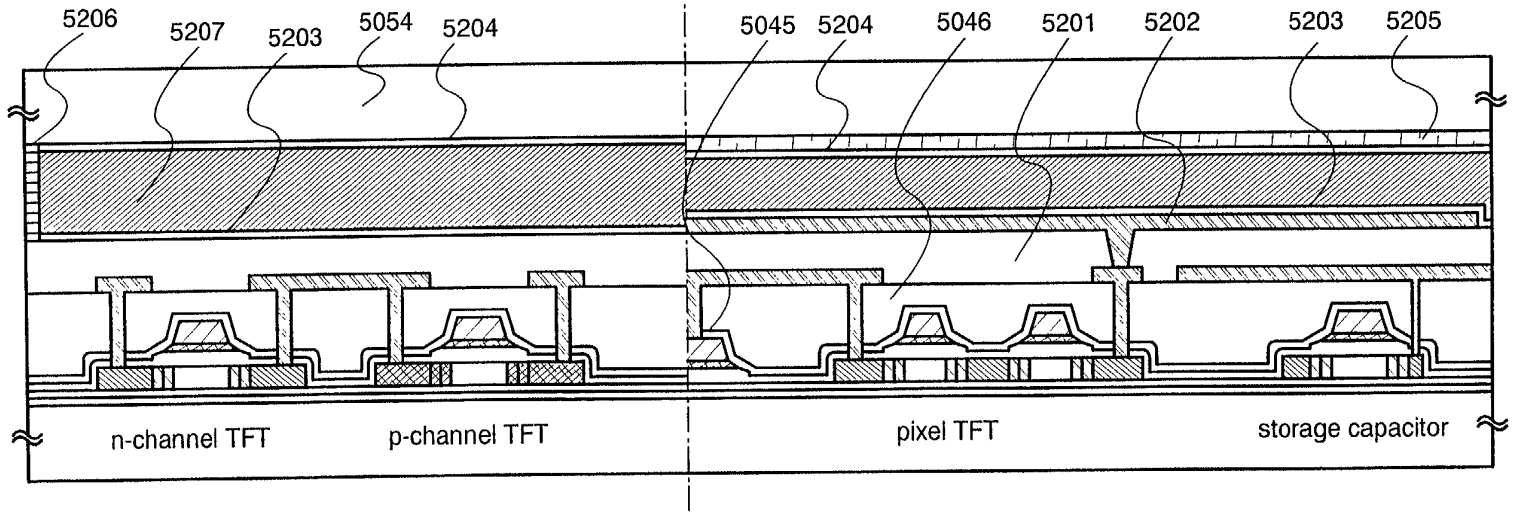


Fig. 20

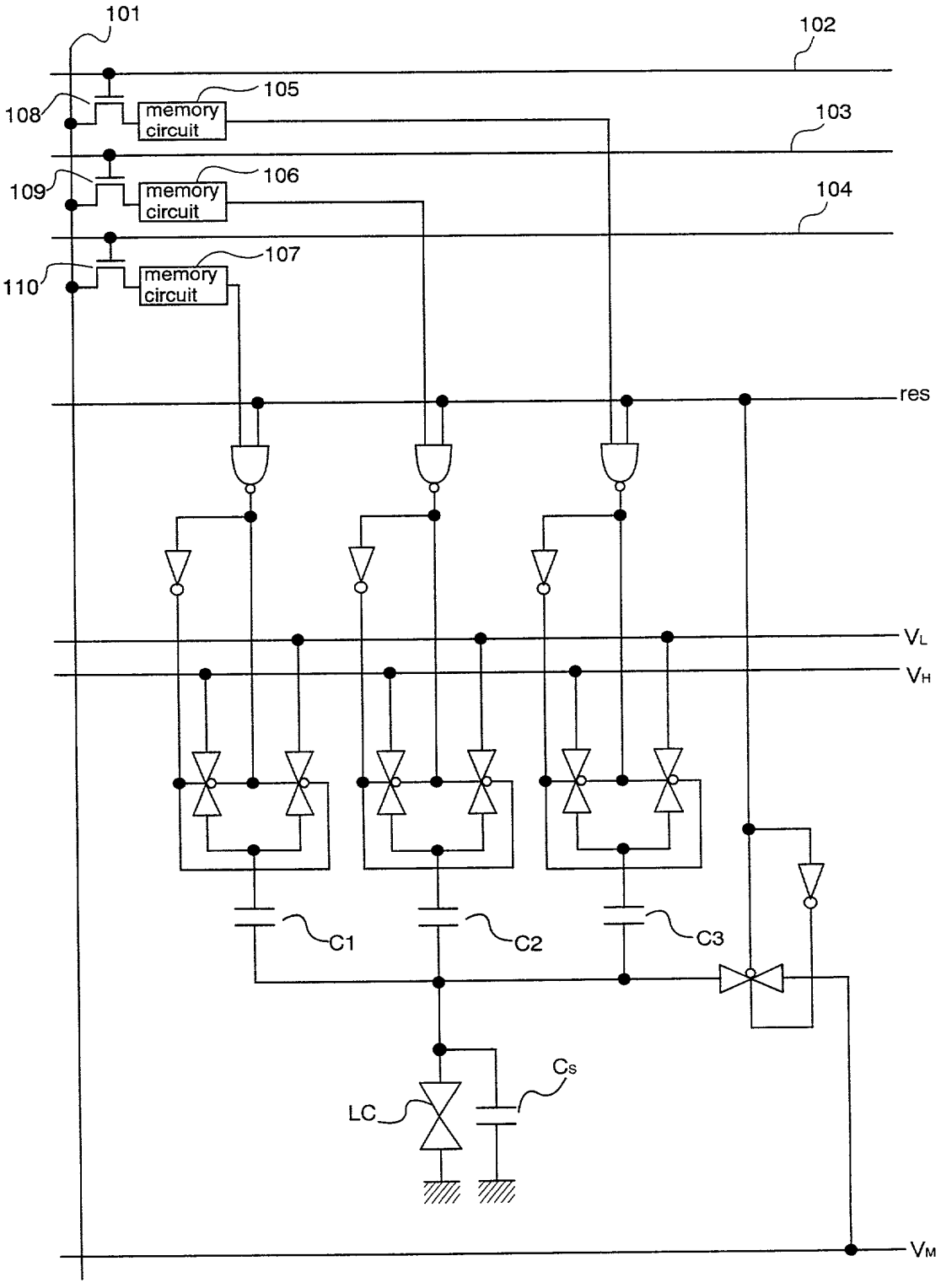

101
102
105
108
memory circuit
103
106
109
memory circuit
104
107
110
memory circuit
res
V_L
V_H
C1
C2
C3
C_S
LC
V_M

Fig. 21

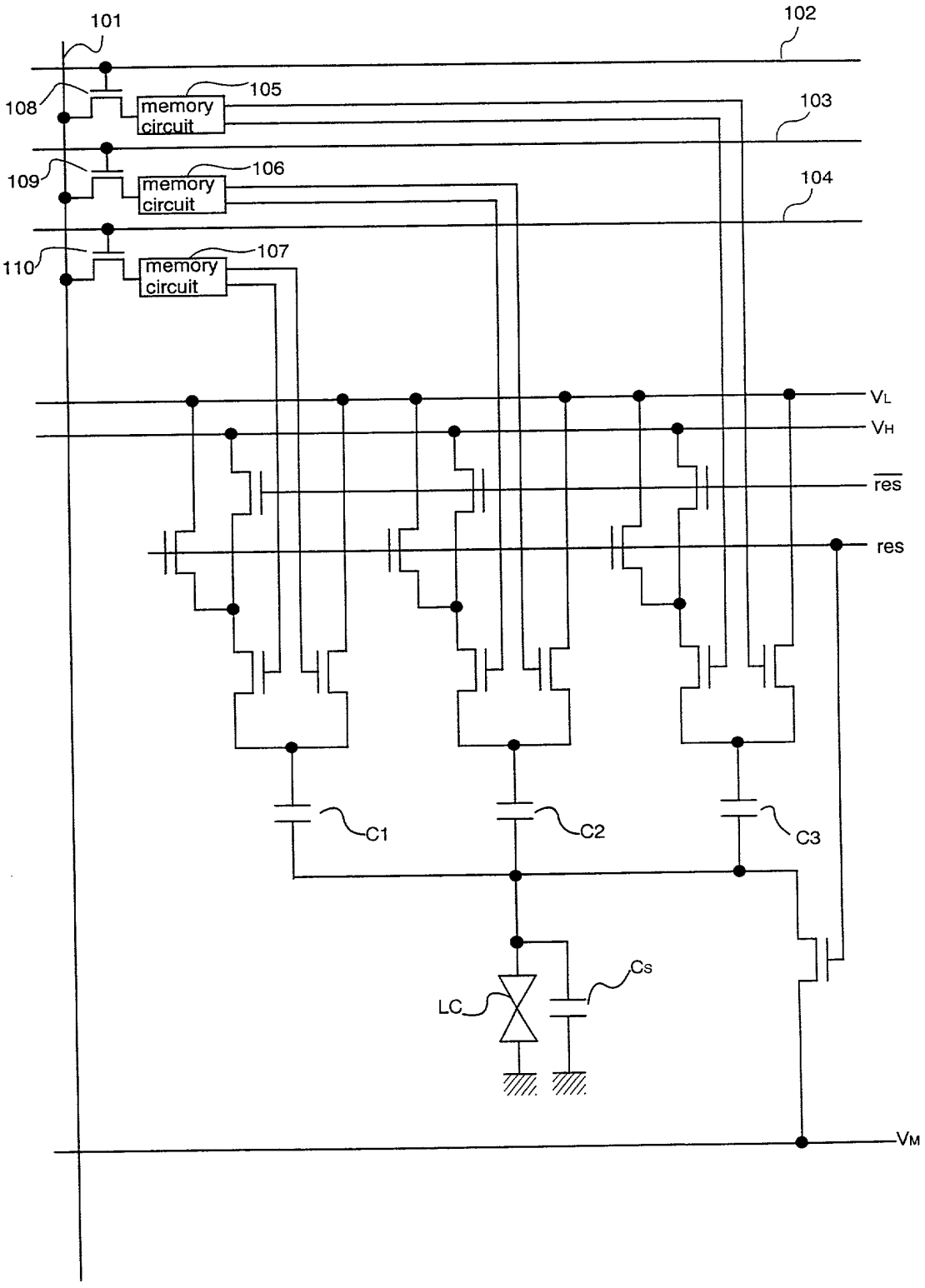

101
102
108
105
memory circuit
103
109
106
memory circuit
104
110
107
memory circuit
VL
VH
res
res
C1
C2
C3
LC
Cs
VM

Fig. 22

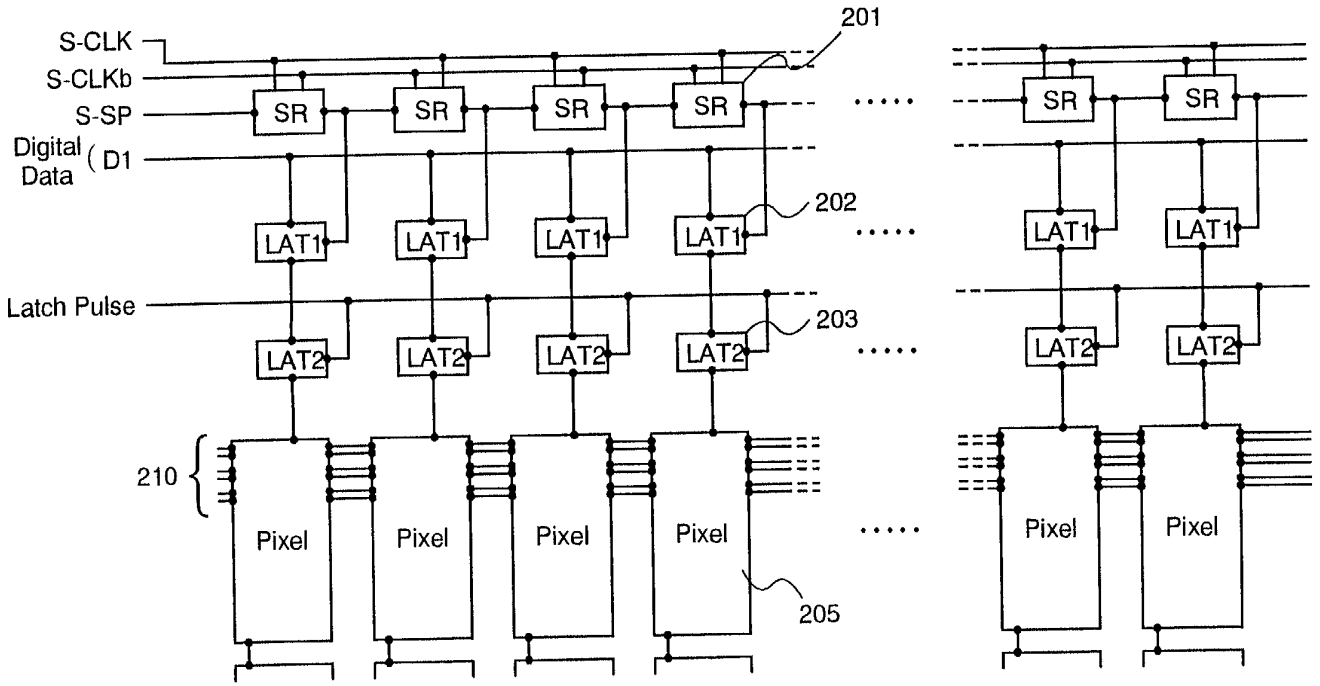

S-CLK
S-CLKb
S-SP
Digital Data (D1
Latch Pulse
201
202
203
205
210
SR
LAT1
LAT2
Pixel

Fig. 23

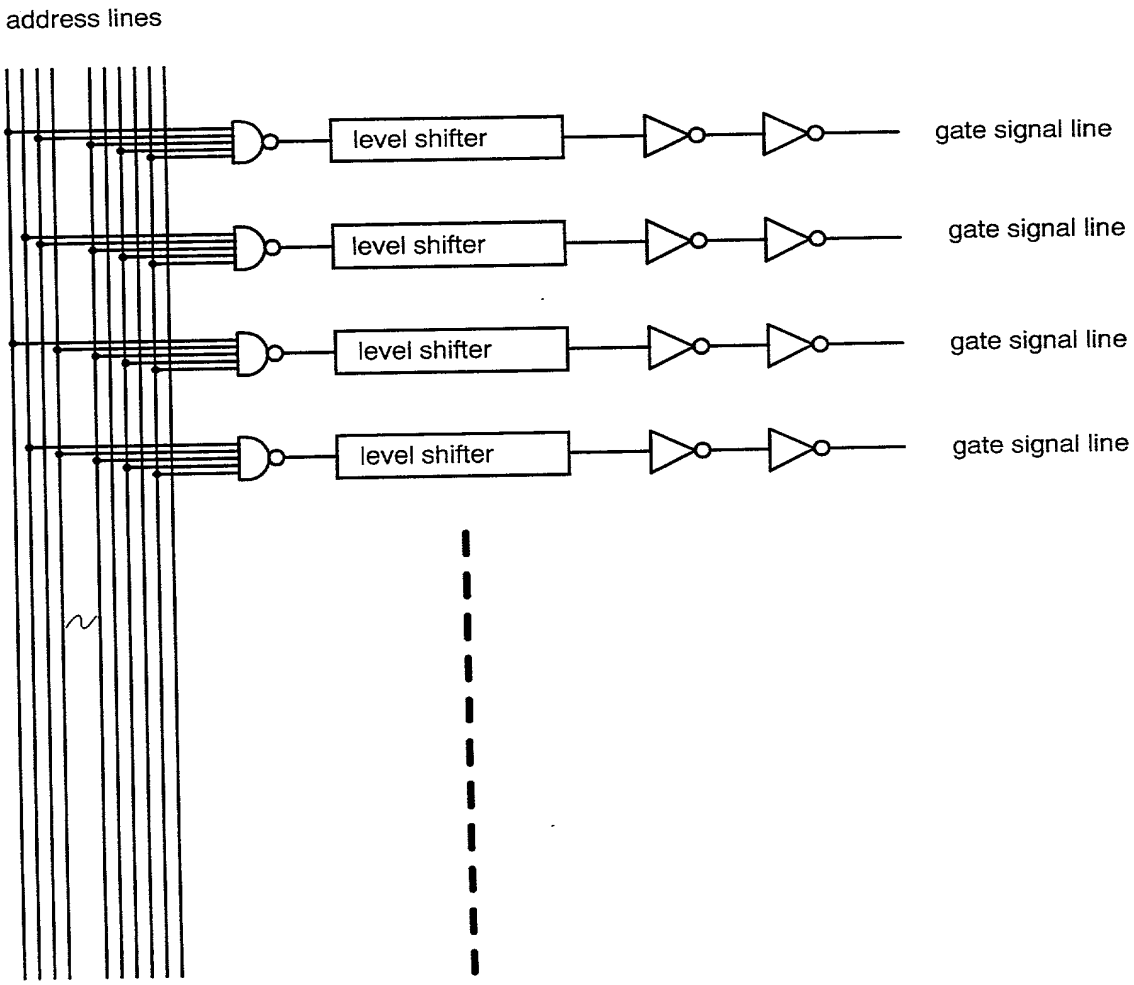

address lines
level shifter
level shifter
level shifter
level shifter
gate signal line
gate signal line
gate signal line
gate signal line

Fig. 24

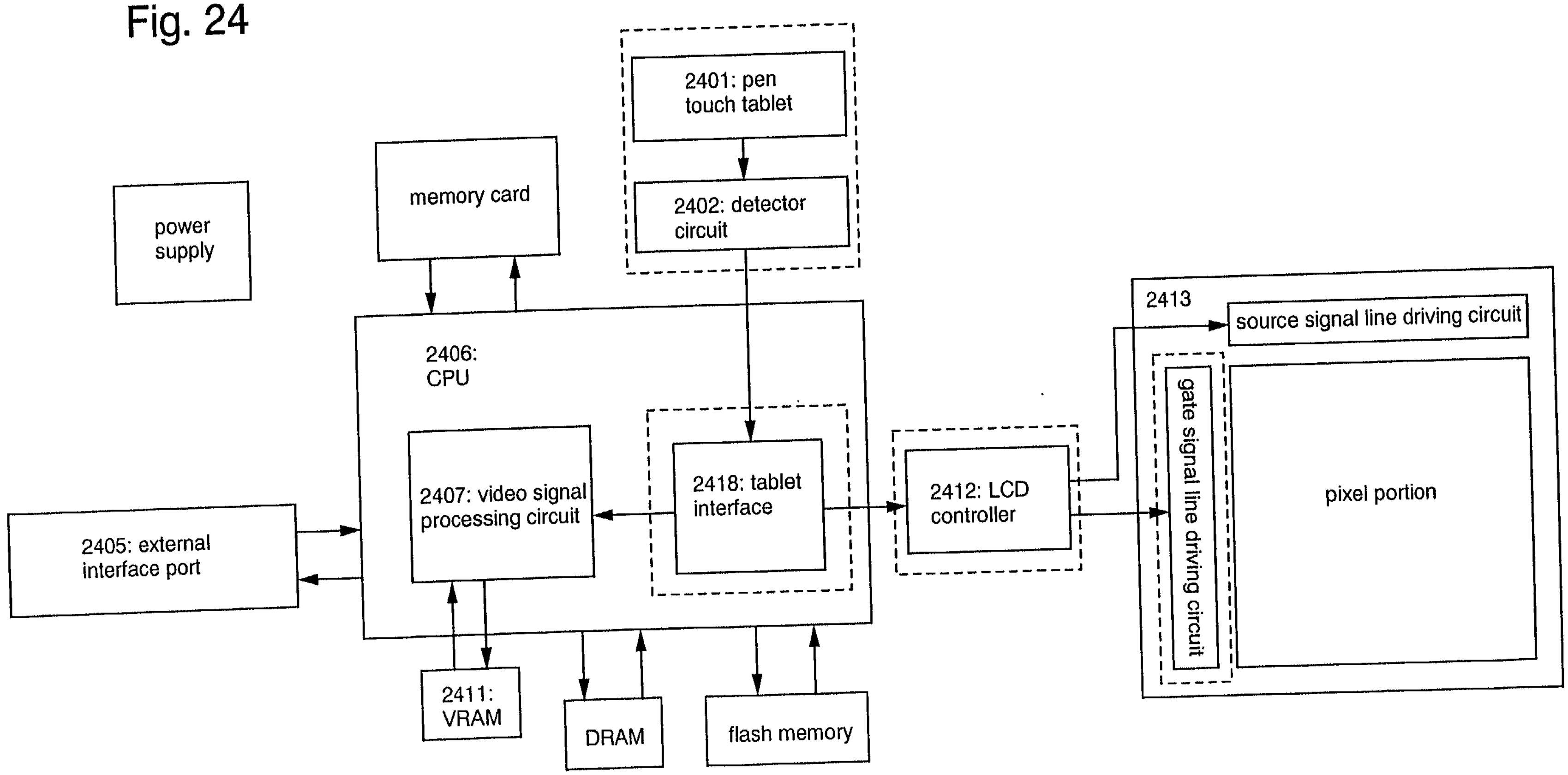

power supply
memory card
2401: pen touch tablet
2402: detector circuit
2406: CPU
2407: video signal processing circuit
2418: tablet interface
2405: external interface port
2411: VRAM
DRAM
flash memory
2412: LCD controller
2413
source signal line driving circuit
gate signal line driving circuit
pixel portion

Fig. 25

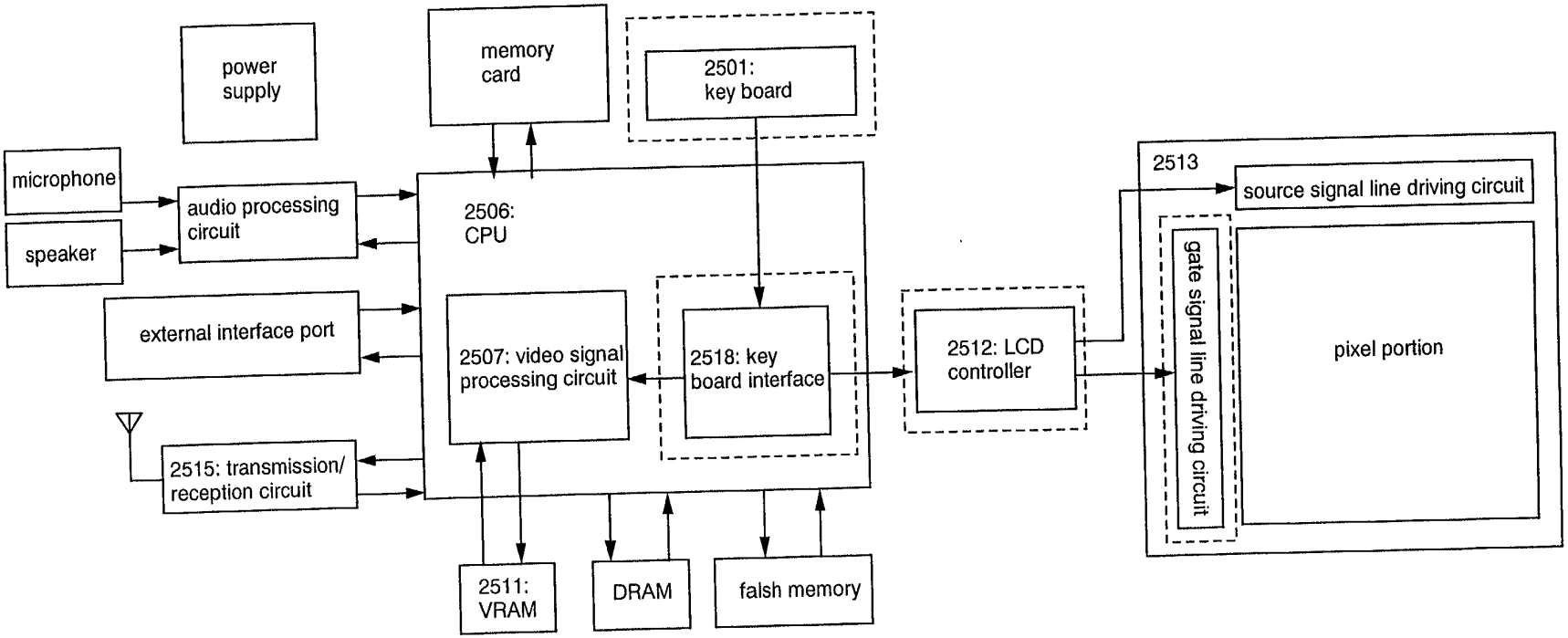


Fig. 26

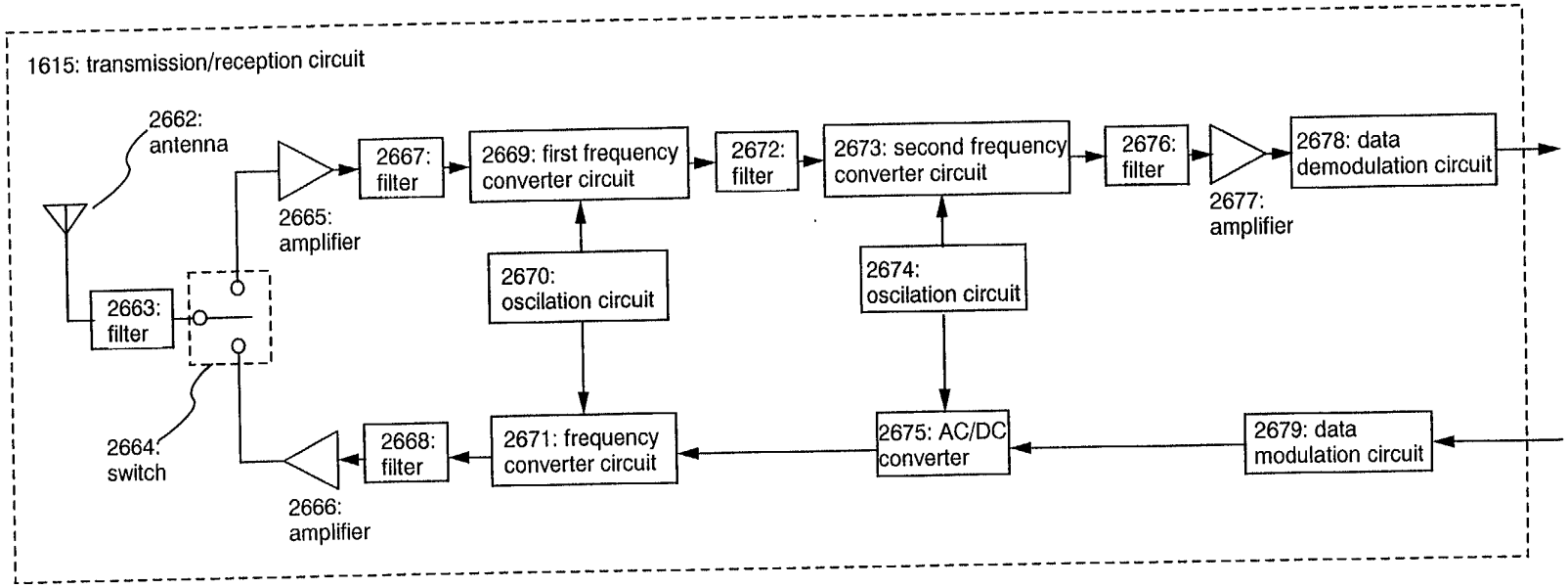

1615: transmission/reception circuit
2662: antenna
2663: filter
2664: switch
2665: amplifier
2666: amplifier
2667: filter
2668: filter
2669: first frequency converter circuit
2670: oscilation circuit
2671: frequency converter circuit
2672: filter
2673: second frequency converter circuit
2674: oscilation circuit
2675: AC/DC converter
2676: filter
2677: amplifier
2678: data demodulation circuit
2679: data modulation circuit

Fig. 27A

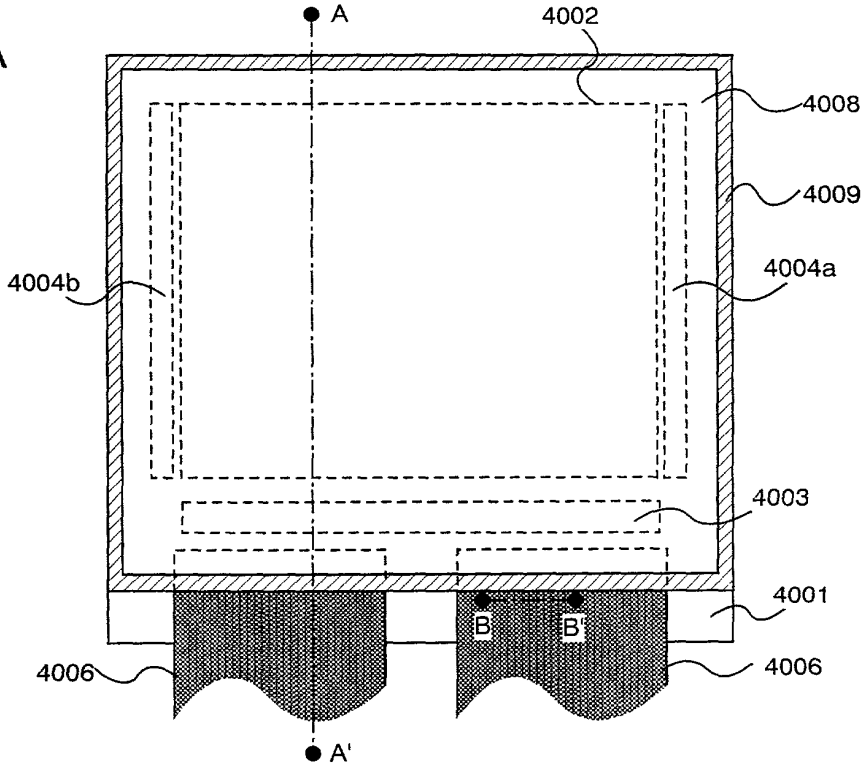


Fig. 27B

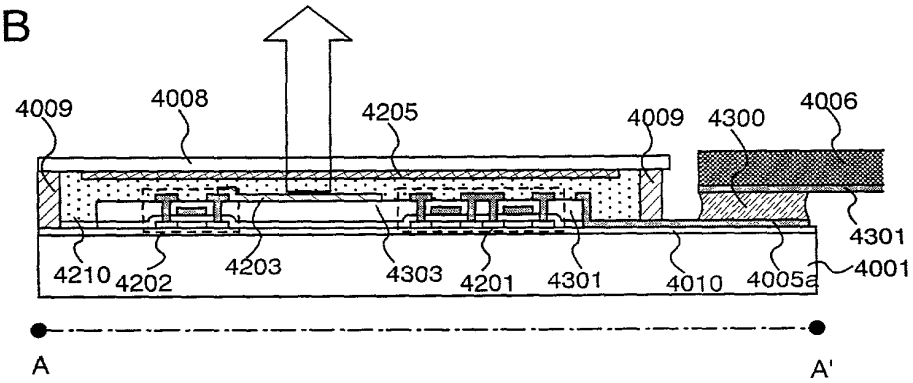
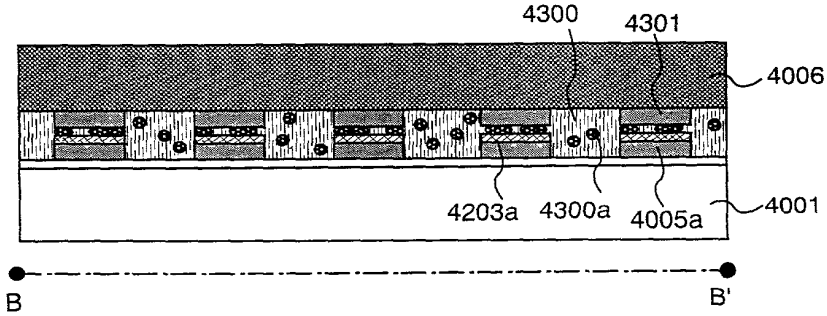


Fig. 27C



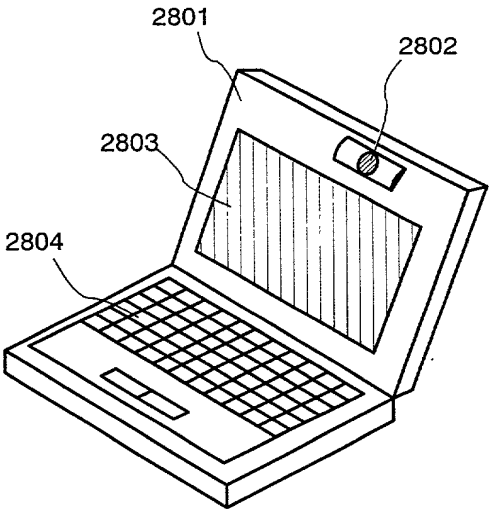


Fig. 28A

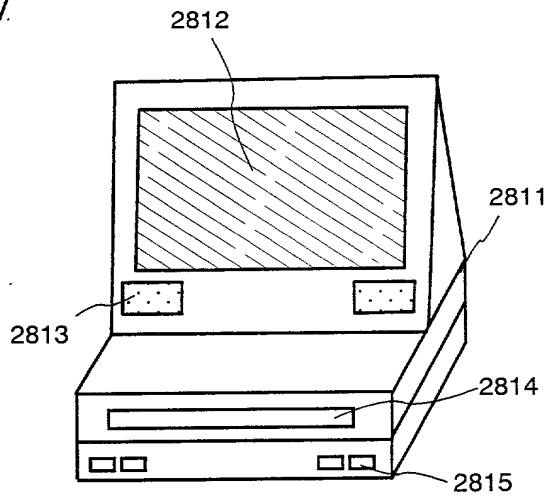


Fig. 28B

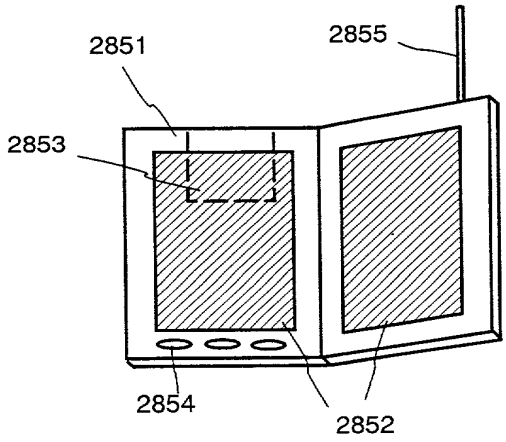


Fig. 28C

Fig. 29A

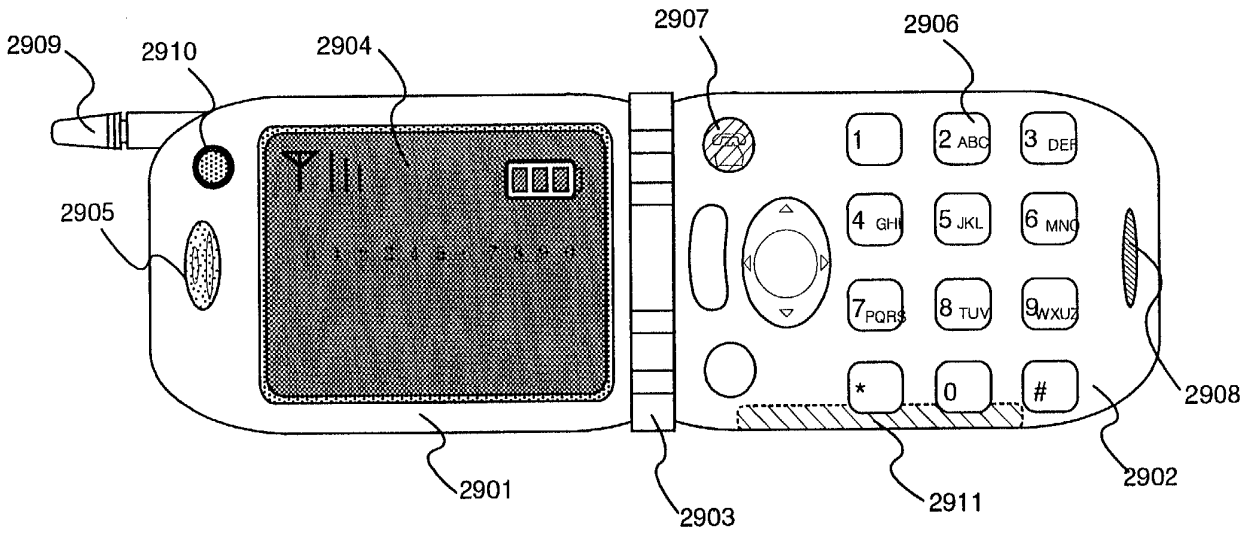


Fig. 29B

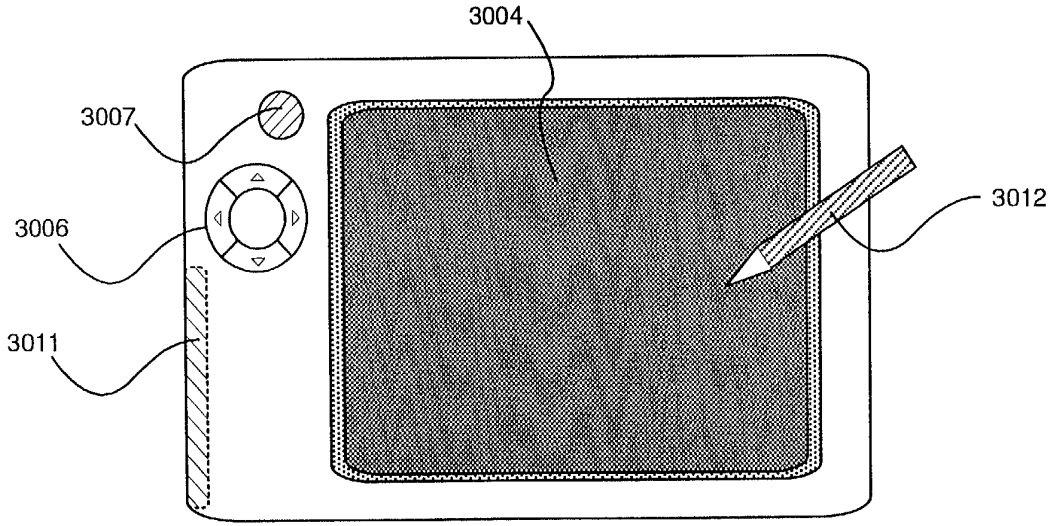


Fig. 30

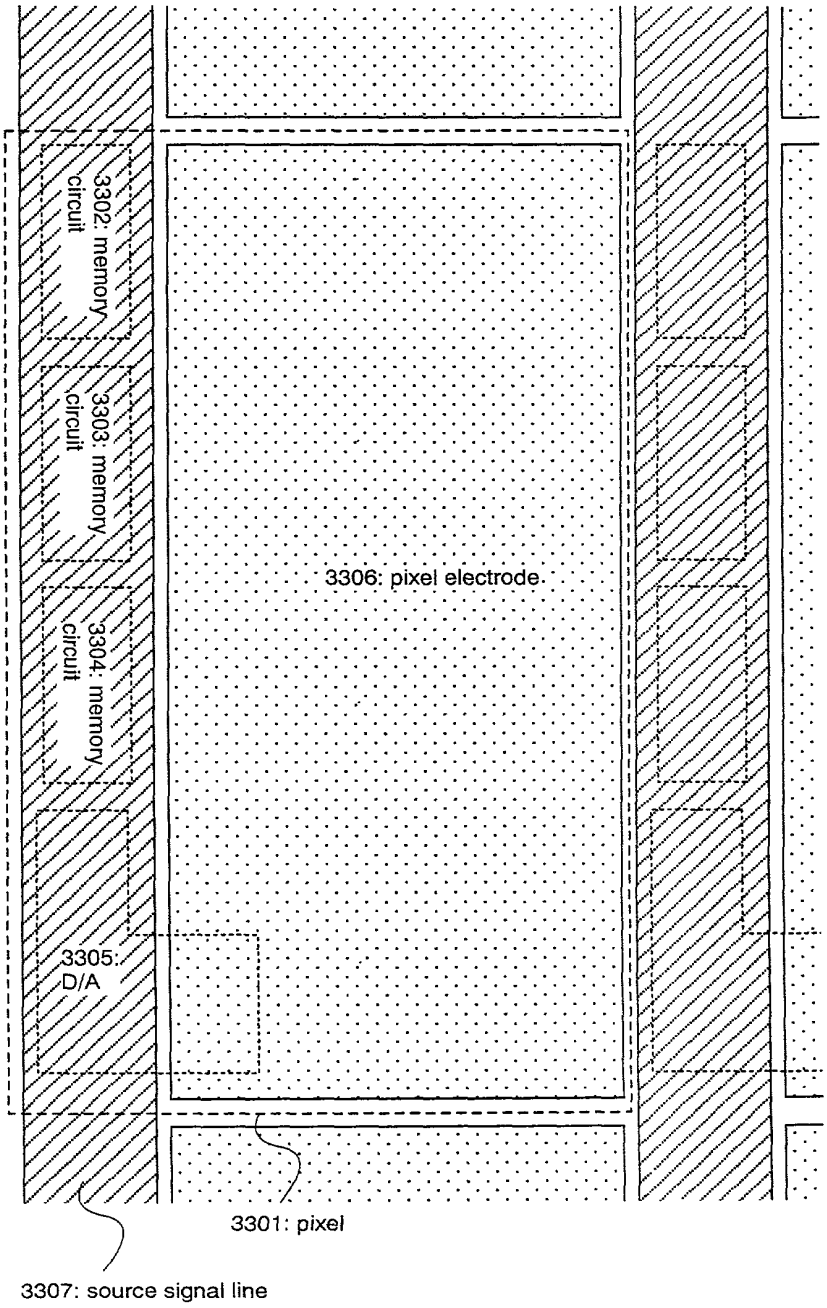

3302: memory circuit
3303: memory circuit
3304: memory circuit
3305: D/A
3306: pixel electrode
3301: pixel
3307: source signal line

Fig. 31

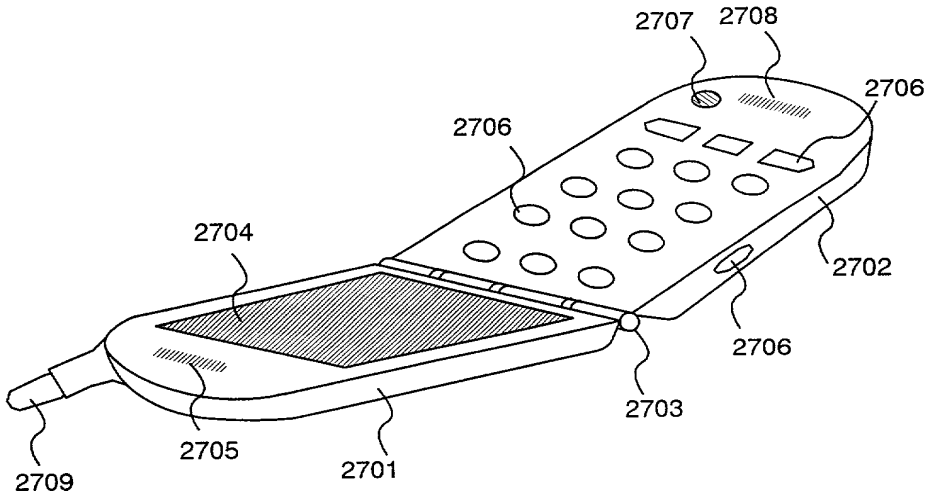


Fig. 32

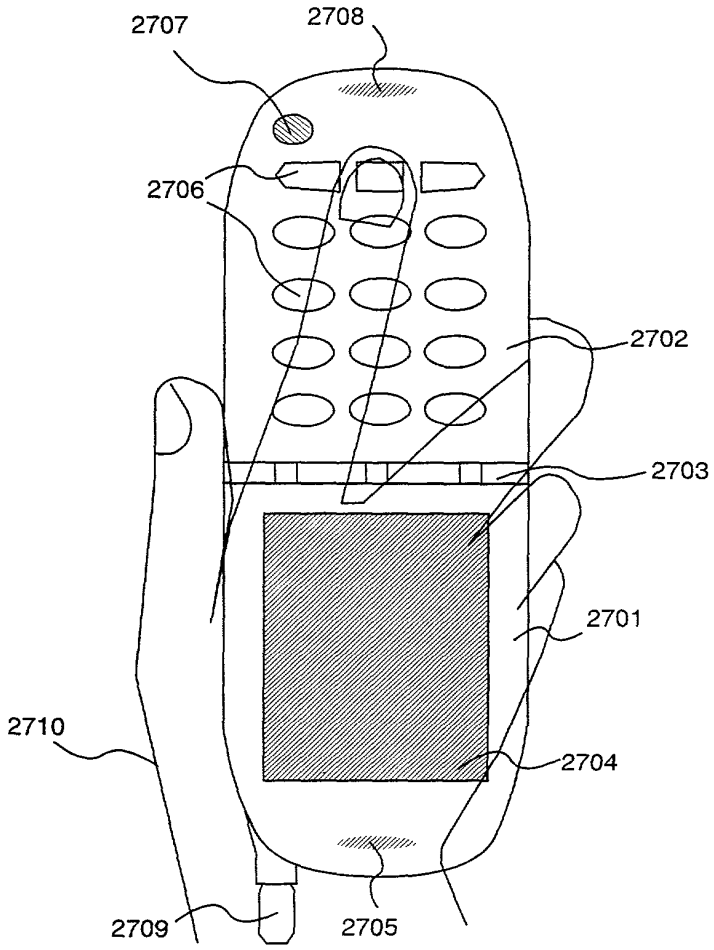


Fig. 33

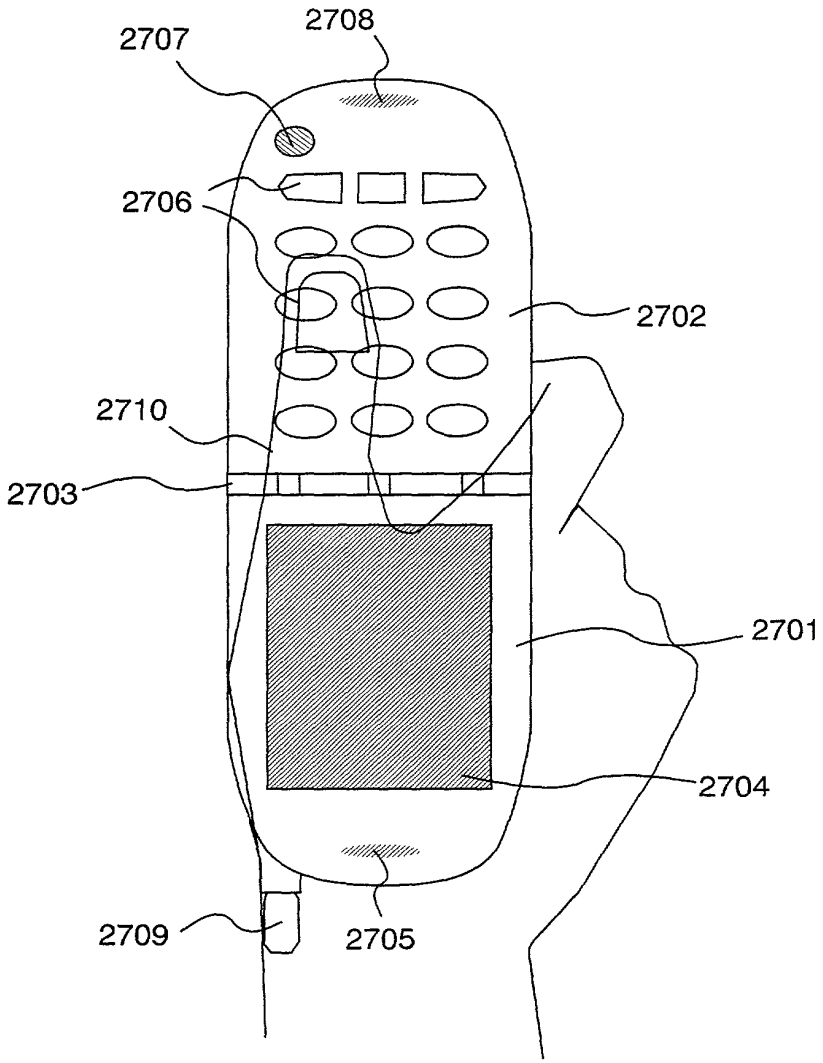


Fig. 34 Prior Art

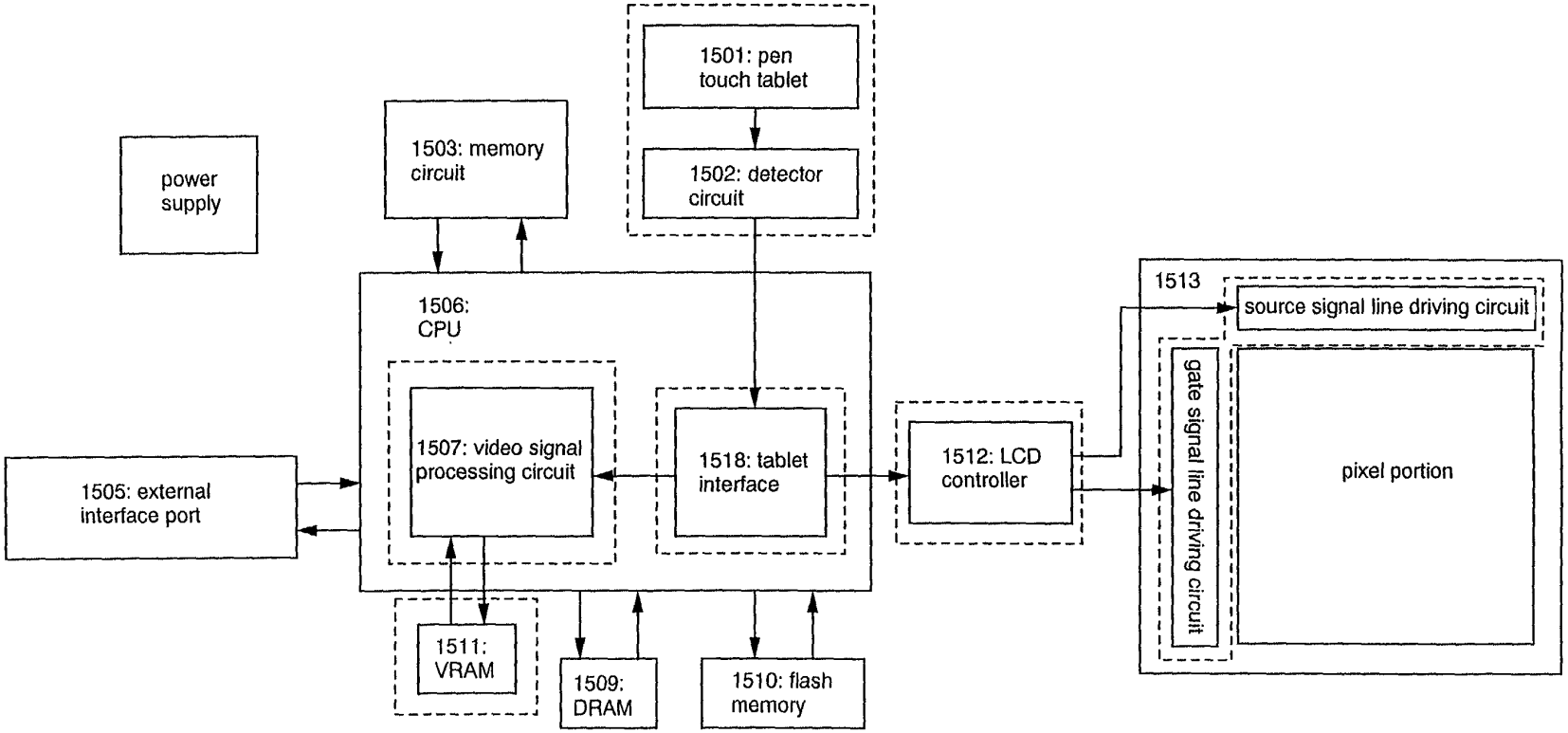


Fig. 35 Prior Art

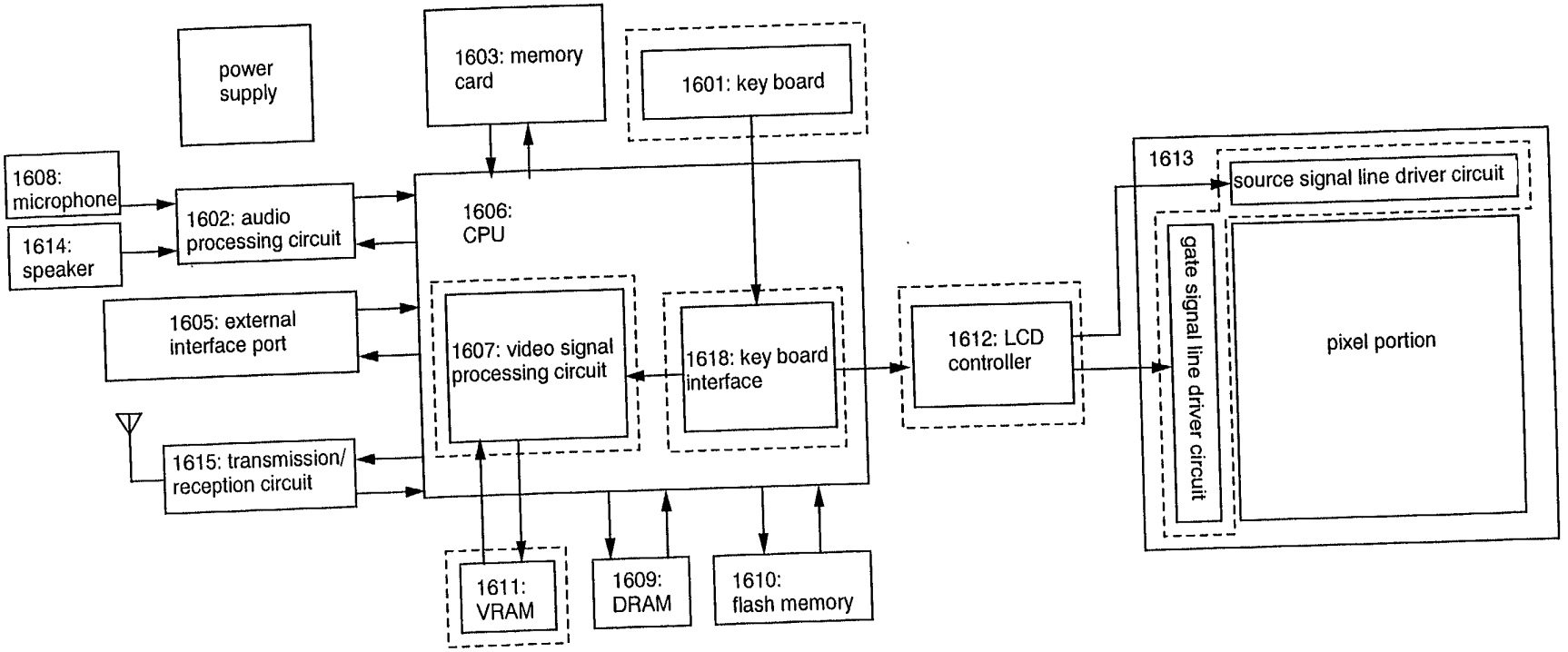


Fig. 36

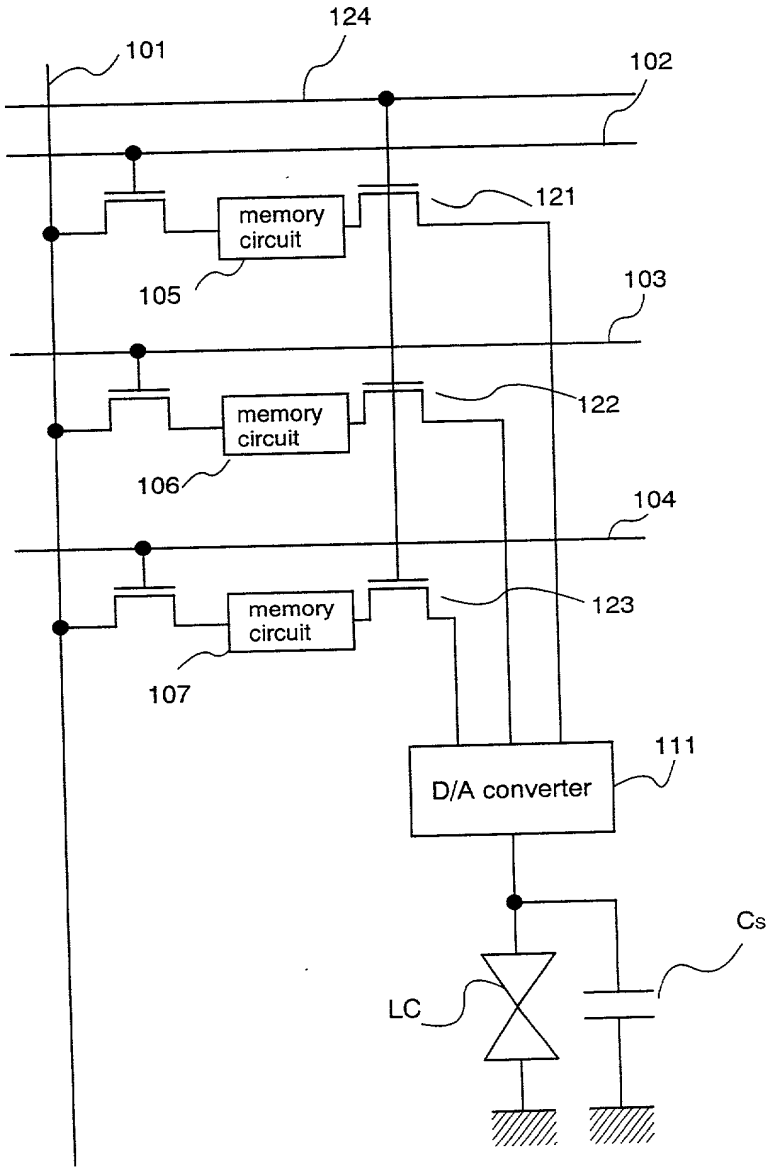

124
101
102
memory circuit
121
105
103
memory circuit
122
106
104
memory circuit
123
107
111
D/A converter
Cs
LC

Fig. 37

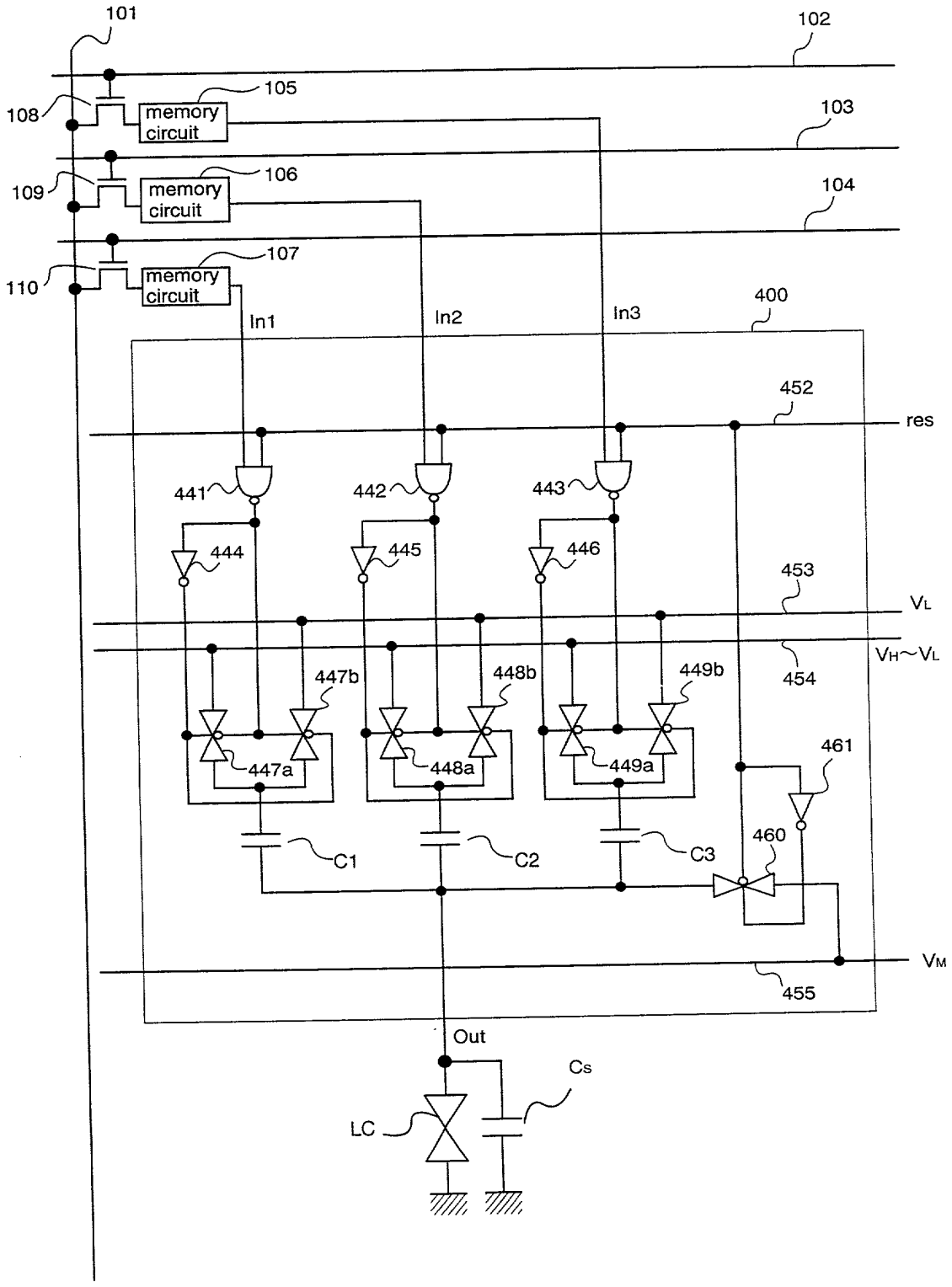
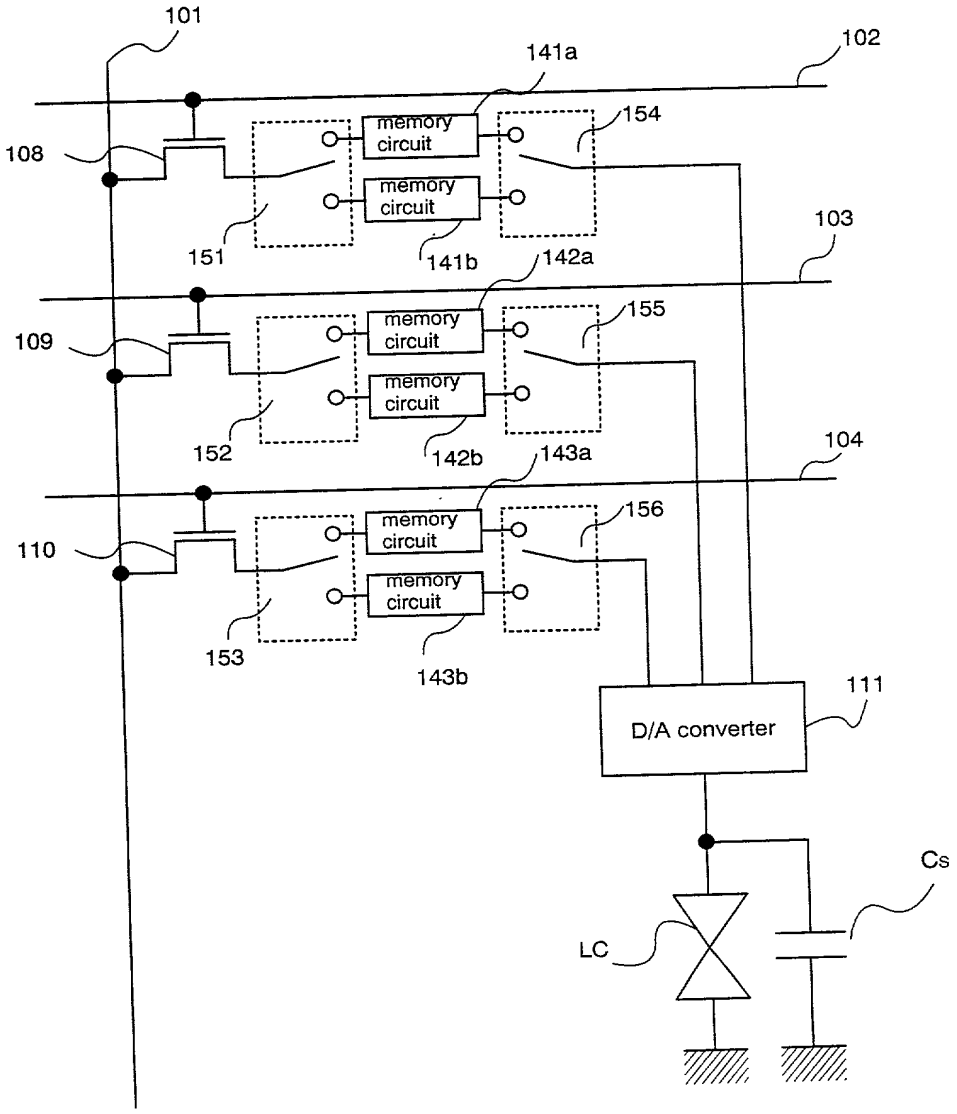

101
102
105
108
memory circuit
103
106
109
memory circuit
104
107
110
memory circuit
In1
In2
In3
400
452
res
441
442
443
444
445
446
453
VL
VH~VL
454
447b
448b
449b
447a
448a
449a
461
460
C1
C2
C3
VM
455
Out
Cs
LC

Fig. 38


101
102
141a
154
memory circuit
memory circuit
108
151
141b
142a
103
155
109
152
142b
143a
104
156
110
153
143b
111
D/A converter
Cs
LC